LpGBT Specifications (Update 18)

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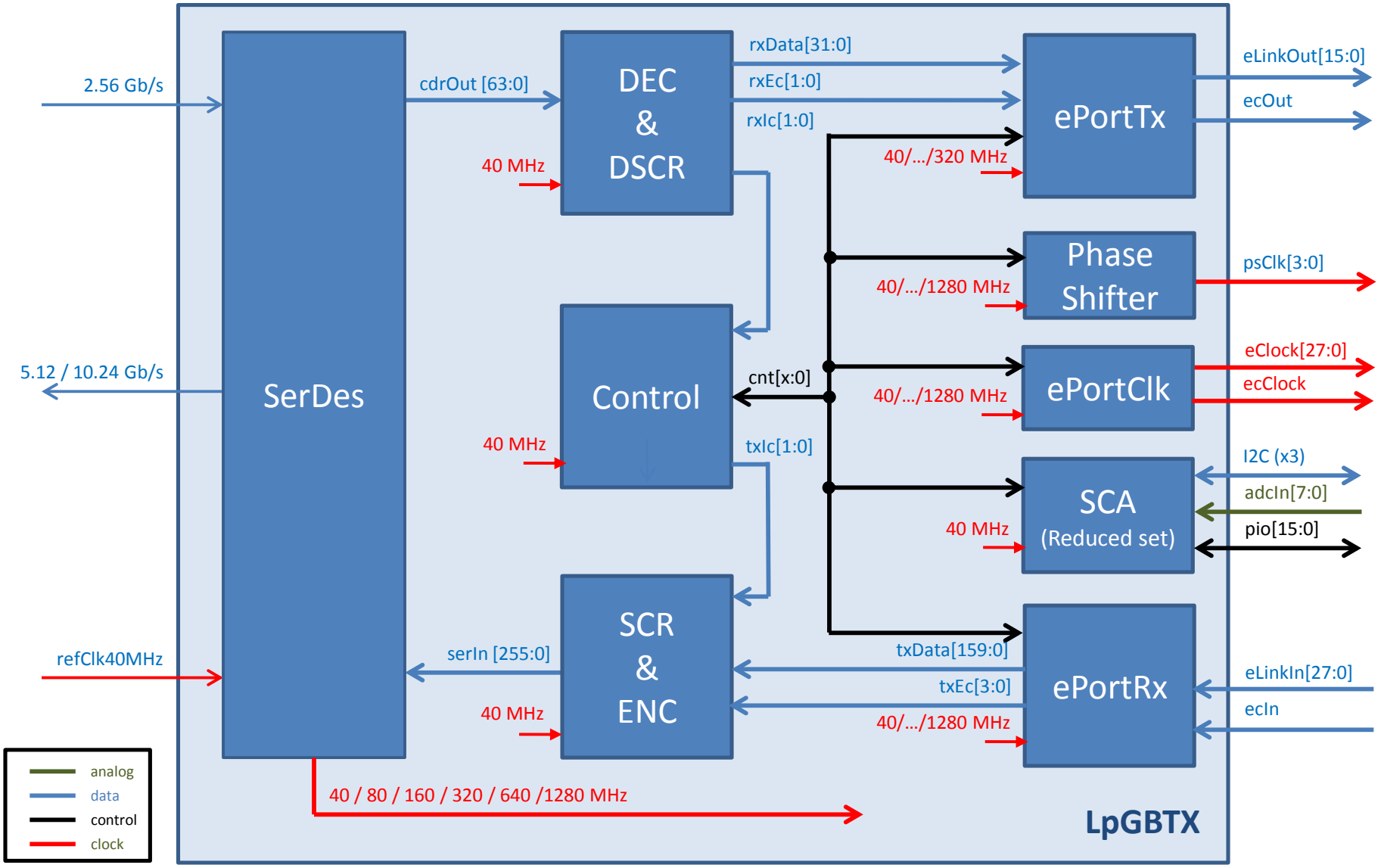
You can find the last update of this document in:
https://espace.cern.ch/GBT-Project/LpGBT/Specifications/LpGbtxSpecifications.pdf

Outline

- LpGBTX Block Diagram
- Main Features:
  - Optical Link
  - E-Links
  - Slow Control
  - Clock Distribution
  - Power Dissipation
  - Radiation Hardness
  - Package
- LpGBT frame and eLinks bandwidth use:
  - Down-Link
  - Up-Link:
    - FEC5
    - FEC12
- eLink – Transmitter / Receiver
- High Speed Line Driver

LpGBTX Block Diagram



Main Features (1/…)

“Optical” link:

- Down-link:
  - 2.56 Gb/s (64 – bit frame)
  - Encoding: FEC12
  - Bandwidth:
    - IC (Internal Control (ASIC control)): 80 Mb/s
    - EC (External Control (SCA e-Link)): 80 Mb/s
    - D (Data): 1.28 Gb/s
  - Eye Scan
  - BER Monitoring based on the FEC activity

Main Features (2/…)

- Up-link:
  - Bandwidth @ 5.12 Gb/s (128 – bit frame):
    - IC: 80 Mb/s
    - EC: 80 Mb/s
    - D:
      - FEC12: 3.84 Gb/s
      - FEC5: 4.48 Gb/s
  - 10.24 Gb/s (256 – bit frame)
    - IC: 80 Mb/s
    - EC: 80 Mb/s
    - D:
      - FEC12: 7.68 Gb/s
      - FEC5: 8.96 Gb/s
  - Programable pre-emphasis

Main Features (3/…)

E-Links:

- Down-link:
  - Bandwidths: 80/160/320 Mb/s
  - Number of links*: 16/8/4
    - "Mirror" function:
      - 80 Mb/s: no;
      - 160 Mb/s: each channel is available on 2 outputs;
      - 320 Mb/s: each channel is available on 4 outputs.
  - One EC channel @ 80 Mbit/s
- Up-Link:
  - FEC5 @ 5.12 Gb/s:
    - Data rate: 160 / 320 / 640 Mb/s
    - # eLinks*: 28 / 14 / 7
  - FEC5 @ 10.24 Gb/s:
    - Bandwidth: 320 / 640 / 1280 Mb/s
    - # eLinks*: 28 / 14 / 7
  - FEC12 @ 5.12 Gb/s:
    - Bandwidth: 160 / 320 / 640 Mb/s
    - # eLinks*: 24 / 12 / 6
  - FEC12 @ 10.24 Gb/s:
    - Bandwidth: 320 / 640 / 1280 Mb/s
    - # eLinks*: 24 / 12 / 6
  - One EC channel @ 80 Mbit/s
  - Phase alignment on a per channel basis:
    - User programable phase
    - Automatic phase tracking

* Excluding the EC channel

Main Features (4/…)

Latency

- Both the RX and TX will have fixed and “deterministic” latency

eLink Line Drivers

- Programable:
  - Driving current: 1, 2 and 4 mA
  - Common mode voltage: 600 mV
  - Receiving end termination 100 Ω
  - Pre-emphasis

eLink Line Receivers

- Programable:
  - 100 Ω differential terminations (on/off)
  - Auto bias for AC coupling (on/off)
  - Line equalization

Main Features (5/…)

ASIC control:

- IC channel: 80 Mb/s
- I2C interface
- EC channel with double role:
  - When the LpGBT works as a Transceiver:
    - The EC channel is used to convey (control) data to and from the GBT – SCA, an ASIC or a frontend module
  - When the LpGBT works as a Simplex Receiver or Transmitter:
    - The EC channel is used as an ASIC control channel (having a similar role and functionality as the IC channel).

Main Features (6/…)

Slow Control:

- LpGLD control:
  - I2C master
- Experiment control:
  - Two I2C masters
  - Programmable parallel port:
    - 16 x DIO
- Environmental monitoring:
  - 10-bit ADC:
    - 8 inputs
  - Temperature:
    - On chip: yes
    - Programable current source to drive an external temperature sensor
- Environmental stimulus:
  - 8 – bit DAC:
    - Single output
    - Range: 0 to 800 mV
    - Noise: < 1 mV
    - DNL: < 1 LSB
    - INL:
      - Full range: < 3 LSB
      - Range 200 to 800 mV: < 1 LSB

Main Features (7/…)

Clock distribution:

- Phase/Frequency – 4 programmable clocks
  - 4 independent
  - Phase resolution: 50 ps
  - Frequencies: 40 / 80 / 160 / 320 / 640 / 1280 MHz
- eLink Clocks:
  - 28 independent
  - Fixed phase
  - Frequency programable
  - Frequencies: 40 / 80 / 160 / 320 / 640 / 1280 MHz
- Clock jitter:
  - < 5 ps rms

Power dissipation:

- 500 mW @ 5.12 Gb/s
- 750 mW @ 10.24 Gb/s

Radiation hardness:

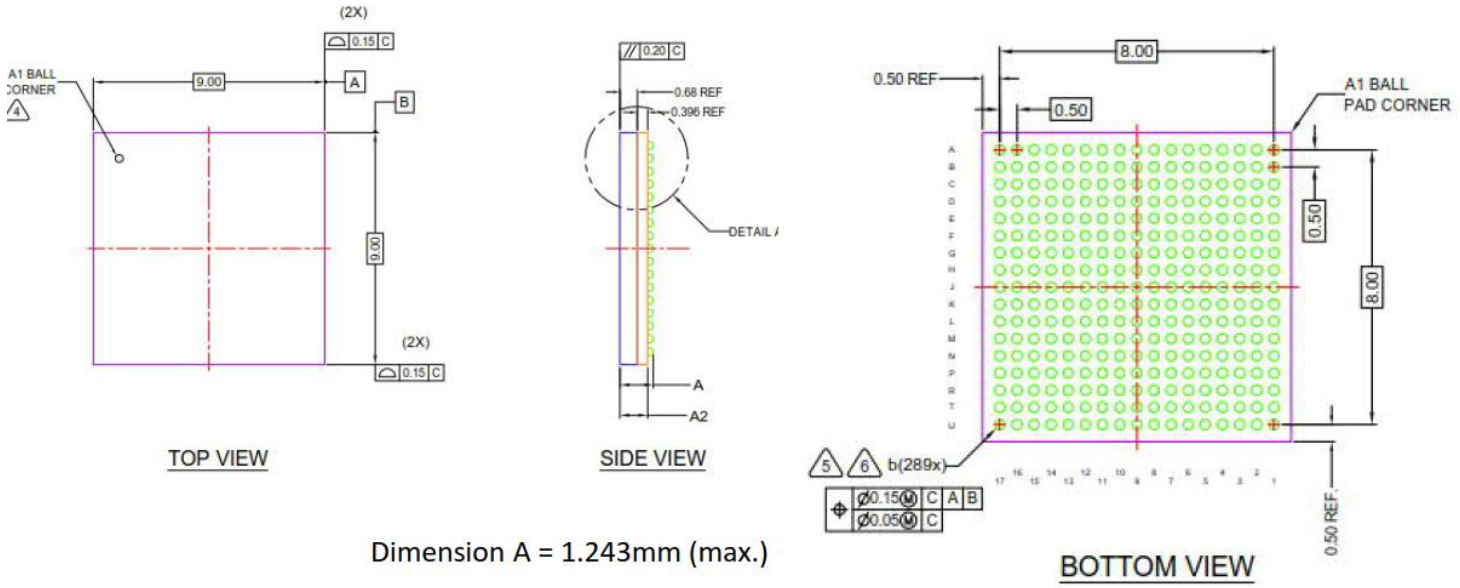
- Total dose:
  - 200 Mrad
- SEU robust

Main Features (8/.)

Package:

- BGA
- Fine Pitch:
  - 0.5 mm
- Pin count:
  - 289 (17 x 17)
- Size:
  - 9 mm x 9 mm x 1.243 mm

DRAFT DIMENSIONS



Dimension A = 1.243mm (max.)

LpGBT Frame and eLinks Bandwidth Use

Downlink

- Single data rate:
  - 2.56 Gb/s
- Frame:
  - IC field:
    - 2 – bit
    - 80 Mb/s
  - EC field:
    - 2 – bit
    - 80 Mb/s
  - Data field:
    - 32 – bit
    - 1.28 Gb/s
  - FEC field:
    - 24 – bit
- Error correction:
  - FEC:
    - Interleaving: 4
    - Symbol width: 3 – bit
    - Number of wrong symbols: 1 (× 4)
  - Up to 12 consecutive bits
  - Efficiency: 56%
- eLinks:
  - Data
    - 16 eLinks @ 80 Mb/s
    - 8 eLinks @ 160 Mb/s
    - 4 eLinks @ 320 Mb/s
  - EC
    - 1 eLink @ 80 Mb/s

Option	37
Frame (bits)	**64**
Header (bits)	**4**
Coded header	**Yes**
User field (bits)	**36**
Code (bits)	24
8-bit multiplicity	4.5
User Bandwidth (GHz)	1.44
# eLinks groups (8 bit)	4
eLinks bandwidth (MHz)	80/160/320
#eLinks	16/8/4
EC bandwidth (MHz)	80
IC bandwidth (MHz)	80
Corrected (bits)	**12**
Efficiency	**56%**

Uplink – FEC 5

- Dual data rate:
  - 5.12 Gb/s
  - 10.24 Gb/s
- Frame:
  - Header:
    - 2 / 4 – bits
    - 2'b10 (high) & 2'b01 (low)
  - IC field:
    - 2 – bit
    - 80 Mb/s
  - EC field:
    - 2 – bit
    - 80 Mb/s
  - Data field:
    - 112 / 224 – bit
    - 4.48 / 8.96 Gb/s
  - FEC field:
    - 10 / 20 – bit
- Error correction:
  - FEC:
    - Interleaving: 1 / 2
    - Symbol width: 5 – bit
    - Number of wrong symbols: 1 (× 1 / × 2)
  - Up to 5 / 10 consecutive bits
  - Efficiency: 91%
- eLinks:
  - Data
    - 28 eLinks @ 160 / 320 Mb/s
    - 14 eLinks @ 320 / 640 Mb/s
    - 7 eLinks @ 640 / 1280 Mb/s
  - EC
    - 1 eLink @ 80 Mb/s

FEC5

	5.12 Gb/s	10.24 Gb/s
Option	7	7
Frame (bits)	**128**	**2 x 128**
Header (bits)	**2**	**2+2**
Coded header	**no**	**no**
User field (bits)	116	232
Code (bits)	10	20
16-bit multiplicity	7.250	14.5
Remainder bits	4	8
User Bandwidth (GHz)	4.64	9.28
# eLinks groups (16 bit)	7	7
eLinks bandwidth (MHz)	160/320/640	320/640/1280
#eLinks	28/14/7	28/14/7
EC bandwidth (MHz)	80	80/160
IC bandwidth (MHz)	80	80/160
Unassigned bits	0	4
Corrected (bits)	**5**	**2 x 5**
Efficiency	**91%**	**91%**

Uplink – FEC 12

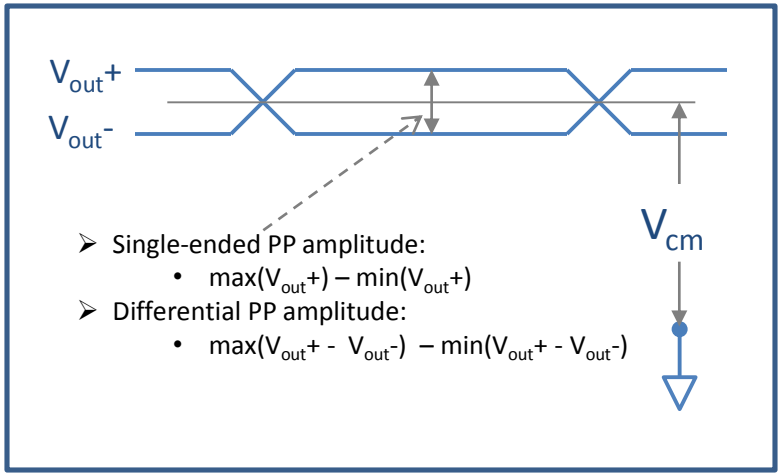
- Dual data rate:
  - 5.12 Gb/s
  - 10.24 Gb/s
- Frame:
  - Header:
    - 2 / 4 – bits
    - 10 (high) & 01 (low)
  - IC field:
    - 2 – bit
    - 80 Mb/s
  - EC field:
    - 2 – bit
    - 80 Mb/s
  - Data field:
    - 96 / 192 – bit
    - 3.84 / 7.68 Gb/s
  - FEC field:
    - 24 / 48 – bit
- Error correction:
  - FEC:
    - Interleaving: 3 / 6
    - Symbol width: 4 – bit
    - Number of wrong symbols: 1 (× 3 / × 6)
  - Up to 12 / 24 consecutive bits
  - Efficiency: 78% (if accounting for the unassigned bits)
- eLinks:
  - Data
    - 24 eLinks @ 160 / 320 Mb/s
    - 12 eLinks @ 320 / 640 Mb/s
    - 6 eLinks @ 640 / 1280 Mb/s
  - EC
    - 1 eLink @ 80 Mb/s

FEC12

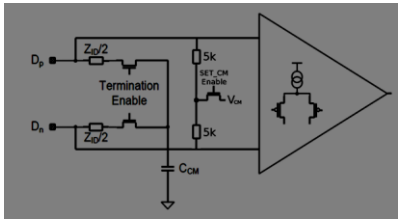
	5.12 Gb/s	10.24 Gb/s
Option	28	28
Frame (bits)	**128**	**2 x 128**
Header (bits)	**2**	**2+2**
Coded header	**no**	**no**
User field (bits)	102	204
Code (bits)	24	48
16-bit multiplicity	6.375	12.75
Remainder bits	6	12
User Bandwidth (GHz)	4.08	8.16
# eLinks groups (16 bit)	6	6
eLinks bandwidth (MHz)	160/320/640	320/640/1280
#eLinks	24/12/6	24/12/6
EC bandwidth (MHz)	80	80/160
IC bandwidth (MHz)	80	80/160
Unassigned bits	2	8
Corrected (bits)	**12**	**2 x 12**
Efficiency	**80%**	**80%**

eLink – Transmitter / Receiver Overview

- Signaling: “CERN Low Power Signaling” (CLPS)
- Down-link Transmitter (eTx):
  - Bandwidths:
    - Data: up to 320 Mb/s
      - To be used as a macro cell the eTx will be designed to support 1.28 Gb/s data transmission
    - Clock: up to 1.28 GHz
  - Programable:
    - Driving current: 1 to 4 mA in 0.5 mA steps
    - Receiving end termination 100 Ω
    - Voltage amplitude in 100 Ω:
      - 100 mV to 400 mV (single-ended PP amplitude)
      - 200 mV to 800 mV (differential PP amplitude)
      - Common mode voltage: 600 mV
    - Pre-emphasis:
      - Driving current: 1 to 4 mA in 0.5 mA steps
      - Pulse width: T_{bit} / 2
- Up-Link Receiver (eRx):
  - Bandwidth:
    - Data: up to 1.28 Gb/s
  - Programable:
    - 100 Ω differential terminations (on/off)
    - Auto bias for AC coupling (on/off)
    - Line equalization
      - Under specification



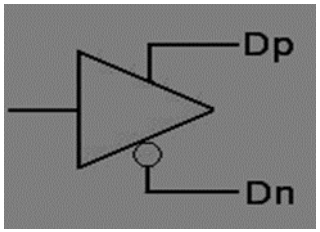
eRx Specification



Parameter	Description	Min	Nom	Max	Units
V_{DD}	Supply voltage range	1.08	1.2	1.32	V
I_{DD}	Average current consumption		850		µA
V_{CMRX}	Common-mode voltage range[A]	70	600	1200	mV
V_{CM}	Common-mode set voltage[B]		$V_{DD}/2$		
$\|V_{ID}\|$	Differential voltage[C]	140	200	450[E]	mV
V_{IDTH}	Differential input[C] high threshold			70	mV
V_{IDTL}	Differential input[C] low threshold	-70			mV
V_{IH}	Single-ended input high voltage		700	V_{DD}+200	mV
V_{IL}	Single-ended input low voltage	-40	500		mV
Z_{ID}	Differential input impedance	80	100	125	Ω
J_R	Random noise jitter			10[F]	ps rms
J_{PW}	Pattern or pulse width dependent jitter[D]			10[F]	ps
$T_{R/F}$	Output rise/fall time		30		ps
PSR	Power supply rejection			10[F]	ps/100mV
CMR	Common mode rejection			10[F]	ps/100mV

[A] Common mode: $(V_{DP} + V_{DN}) / 2$
[B] For AC coupled signals
[C] Differential voltage: $V_{DP} - V_{DN}$
[D] Change of delay through the receiver with PRBS 2^{12}-1 @ 1.28Gbit/s or varying pulse width T_{PW} > 1ns
[E] For LVDS: 400mV
[F] If <=1ps possible (even with reduced input range), receiver could be used as hit receiver

eTx Specification



Parameter	Description	Min	Nom	Max	Units
V_{DD}	Supply voltage range	1.08	1.2	1.32	V
V_{CMTX}	Common-mode voltage[A,B]	430	600	770	mV
$\lvert\Delta_{VCMTX(1,0)}\rvert$	VCMTX mismatch when output is Differential-1 or Differential-0			5	mV
$\lvert V_{OD}\rvert$	Differential voltage[B,C]	140	200	270	mV
$\lvert\Delta V_{OD}\rvert$	VOD mismatch when output is Differential-1 or Differential-0			10	mV
V_{OH}	Single-ended output high voltage[B]		700	900	mV
V_{OL}	Single-ended output low voltage[B]	300	500		mV
I_{MOD}	Modulation output current [D]	0.7	1 to 4	5.4	mA
I_{PRE}	Pre-emphasis output current [D]	0.7	1 to 4	5.4	mA
Z_L	Load impedance		100		Ω

[A] Common mode: $(V_{DP} + V_{DN}) / 2$.
[B] Value when driving into differential load impedance 100 Ω. Termination load is external.
[C] Differential voltage: $V_{DP} - V_{DN}$,values for 2mA setting, scales accordingly for other currents.
[D] Modulation and pre-emphasis currents are programable in 0.5 mA steps from 1 mA to 4 mA. Default setting for the LpGBT is 2mA.

5 - 10 Gb/s Line Driver Specifications

#	Specification	Min	Typ	Max	Unit	Notes
1.1	Supply Voltage		1.2		V	
1.2	Supply Current		40		mA	
1.3	Input Swing	0.2		0.8	V	Differential
1.4	Output Swing	0.2		0.6	V	Differential, programmable
1.5	Emphasis Magnitude	0		10	dB	Programmable
1.6	Rise/Fall Time			40	ps	
1.7	Random Jitter			1.2	ps	
1.8	Deterministic Jitter			20	ps	