CMS TRACKER
PHASE 2 UPGRADE
IT SERVICES V2020
UNDER PROGRESS

INTRODUCTION TO THE SYSTEM

The latest geometry with cabling in tkLayout is IT701. Since the last document (2019) there was a change in the geometry of the TFPX disks. This has basically no effect on the services since there have always been independent per ring. The new TFPX dees will be made alike the TEPX i.e. each dee will have an odd and an even side and two dees will be composing a disk aka double dee.

This update has been imported to tklayout by G. Hugo for illustration reasons and to avoid confusion in the future:

http://ghugo.web.cern.ch/ghugo/layouts/it_cabling/OT800_IT701_cabling/layoutpixel.html

Some notes on this tklayout geometry (IT701) :

- the exact PHI placement of the modules on the TFPX dees on this tklayout version is not the latest one and should be updated for physics studies (no impact on services)
- Black corresponds to TFPX R1 and TBPX L1/2 which are locations that could be potentially using 1x2 3D sensor modules.
- Green corresponds to 1x2 planar modules, orange corresponds to 2x2 planar modules, brown (TEPX D4R1) is dedicated to BRIL.

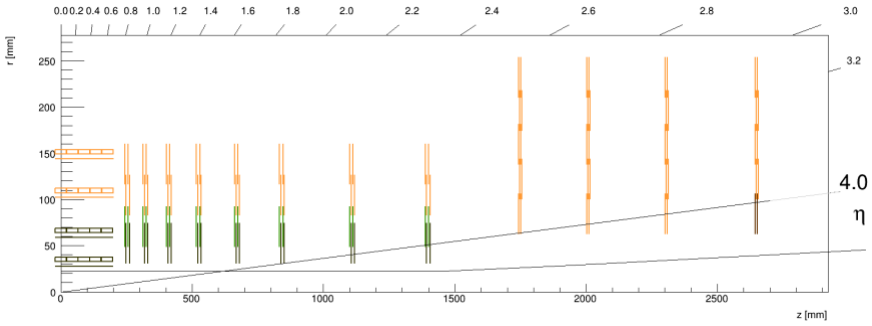


Figure 1. The IT geometry IT701 with the new TFPX dee composition.

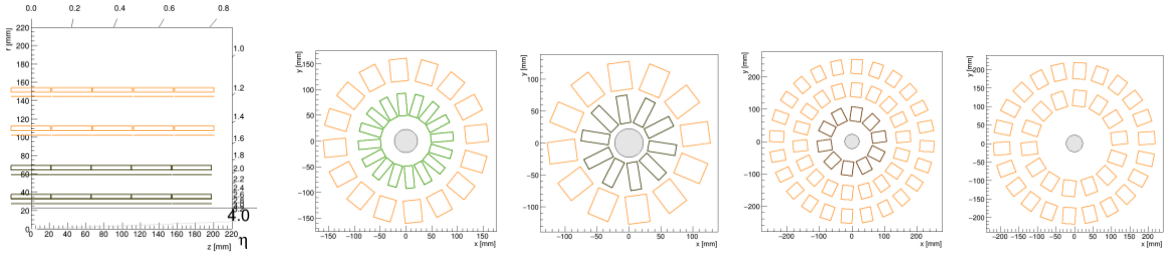


Figure 2. Illustration of the TBPX ladders for a quarter of the detector and the two sides of a TFPX and TEPX dee.

Another major update in 2020 was the new design of the portcard hosting three (instead of previously two) LpGBT chips together with three VTRx+. The portcards will be powered independently by a two stage DC-DC converter scheme located on these boards. The portcards will be installed at locations in the outer radius of the system (known as cartridge), since the optoelectronics have limited tolerance to radiation. In 2020, the location of the TBPX portcards was decided to be between TFPX Disks 6-7 leading to a max length of e-links of 1.6m (plus a margin 10%).

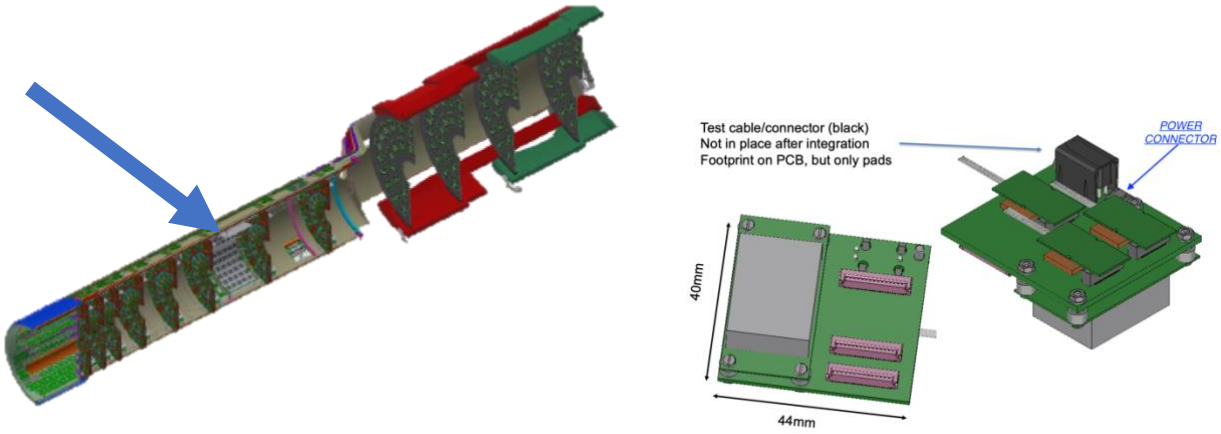


Figure 3. (Left) TBPX portcards will be installed between TFPX Disk 6-7 (see arrow). (Right) The new portcard design featuring 3 vtrx+ (green objects to the right), 3 lpgbts (brown chip below vtrx), 3 elink connectors (pink connectors) and a DCDC mezzannine (grey box is the shielding for the bpols).

An important aspect of the CMS IT design is the choice of serial powering scheme for the pixel modules. The serial powering scheme dictates the grouping of the modules in serial power chains and no crossing of the readout or the sensor biasing is allowed among modules that belong to different chains. A portcard is allowed to readout only modules belonging to the same chain. Given that the modules' reference levels differ along the chain, the e-links are AC-coupled at both the module (command stream) and the portcard side (data stream). Another important update of 2020 is the redesign of the multiservice cables and power supplies (backend) such that they include all the powering needed for the system needs (constant current for a chain, high voltage for sensor bias, portcard powering and the power needed for the preheaters installed at the bulkhead).

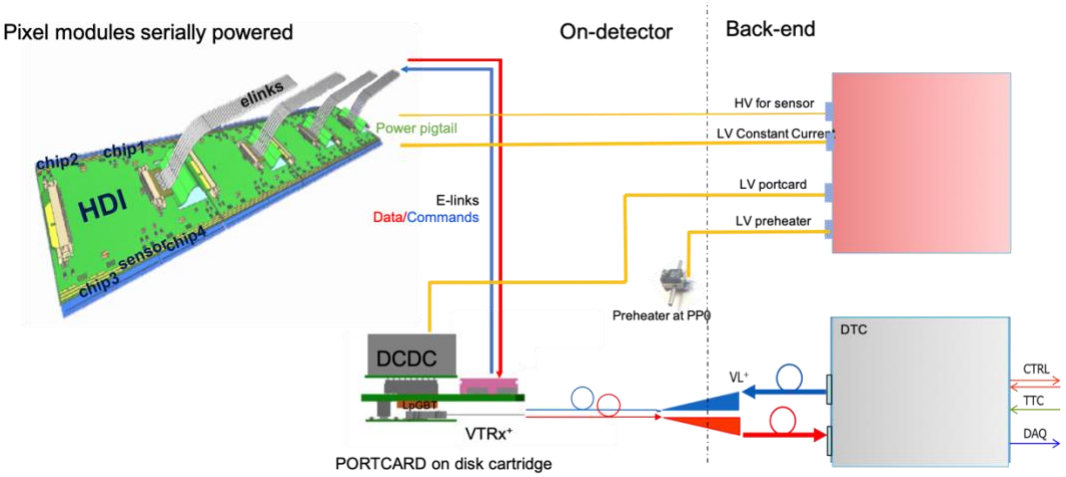


Figure 4 The electronics system architecture.

Table 1. Type of modules and multiplicities of ladders and disks for a quarter of a detector.

QUARTER		Multiplicity (#ladders, #disks)	#modules/ladder		Type of modules	Chips per module	Number of modules		Number of chips	
			Z+	Z-			Z+	Z-	Z+	Z-
BARREL										
TBPX	L1	6	5	4	2x1	2	30	24	60	48
	L2	12	4	5	2x1	2	48	60	96	120
	L3	10	5	4	2x2	4	50	40	200	160
	L4	14	4	5	2x2	4	56	70	224	280
	4 layers SUM						**184**	**194**	**580**	**608**
DISKS			#modules/half disk	#modules/face of dee						
TFPX	R1	8	10	5	2x1	2	80		160	
	R2	8	16	8	2x1	2	128		256	
	R3	8	12	6	2x2	4	96		384	
	R4	8	16	8	2x2	4	128		512	
	Odd dee		22				176		544	
	Even dee		32				256		768	
	1/2 disk		**54**							
	8 1/2 disks SUM						**432**		**1312**	
TEPX	R1	4	10	5	2x2	4	40		160	
	R2	4	14	7	2x2	4	56		224	
	R3	4	18	9	2x2	4	72		288	
	R4	4	22	11	2x2	4	88		352	
	R5	4	24	12	2x2	4	96		384	
	Front side		52	26			208		832	
	Back side		36	18			144		576	
	Dee									
	1/2 disk		**88**							
	4 1/2 disks SUM						**352**		**1408**	
QUARTER OF TBPX+TFPX							616	626	1892	1920
QUARTER OF TEPX							352		1408	
QUARTER OF IT							968	978	3300	3328
ONE END OF IT							1936	1956	6600	6656
ENTIRE IT							**3892**		**13256**	

SERIAL POWERING OF THE MODULES

Each pixel chip will consume about ~2 A and need a supply voltage of 1.5V. (See appendix at the end for chip power). The CMS pixel chip size is shown in the picture below together with the top view of RD53A demonstrator (chip size 20 mm x 11.8 mm). The power consumption of the chip at max. hit/trigger rate, including any SLDO losses (meaning current shunted by the SLDO) is expected to be < 1 W/cm^2.

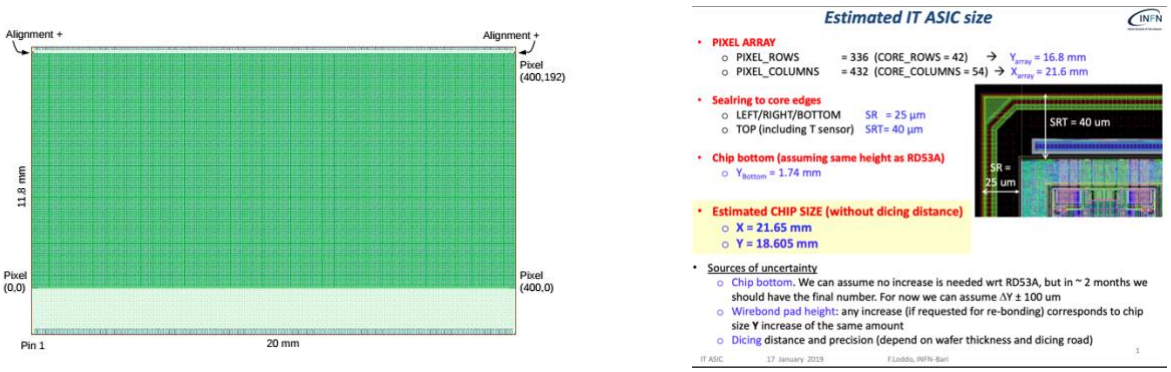


Figure 5. Top view of RD53A pixel array. The width is 20 mm and 400 pixels and the height is 11.8 mm and 192 pixels. The final CMS chip will be an enlarged version of this - right screenshot from https://indico.cern.ch/event/785024/contributions/3265592/attachments/1780471/2896370/CHIP_SIZE_17Jan2019.pdf

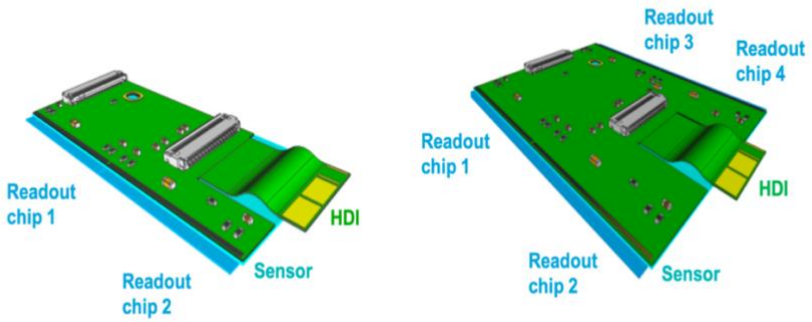


Figure 6. Sketch of the 1x2 and 2z2 pixel modules

Serial power loops feed the required supply current to chains of 5-12 pixel modules, with the two or four pixel chips on each module connected in parallel. Tests with the RD53A chip have shown that power chains of 12 modules can be supported without any issues. Hence the maximum of 10 modules has increased to 12 such that the serial power chains on the rings follow the rule: 1 chain per ring, covering even the longest ring (TEPX R5 12 modules).

TBPX

The guideline of max. 12 modules per chain is translated into TBPX by serially powering every two ladders leading to 8-module chains for the short end and 10-module chains for the long end of the layers. It is straightforward to calculate the chains in the barrel #SPchains= #ladders/2.

TBPX L1 TBPX L2 TBPX L3 TBPX L4

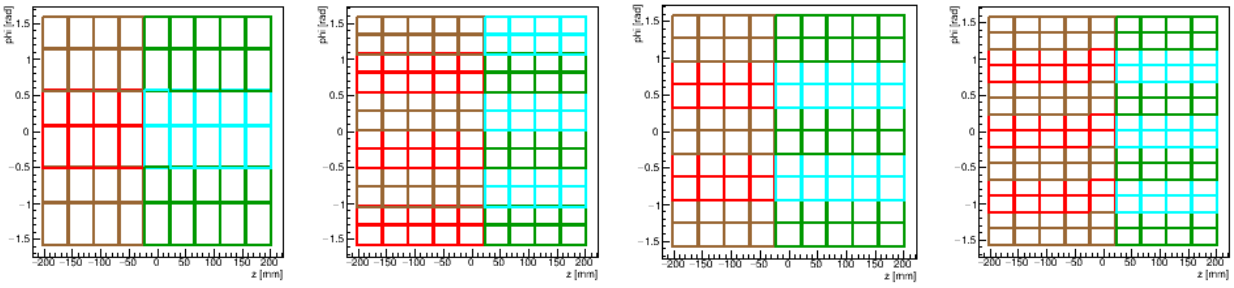


Figure 7

TBPX Z- TBPX Z=0 TBPX Z+

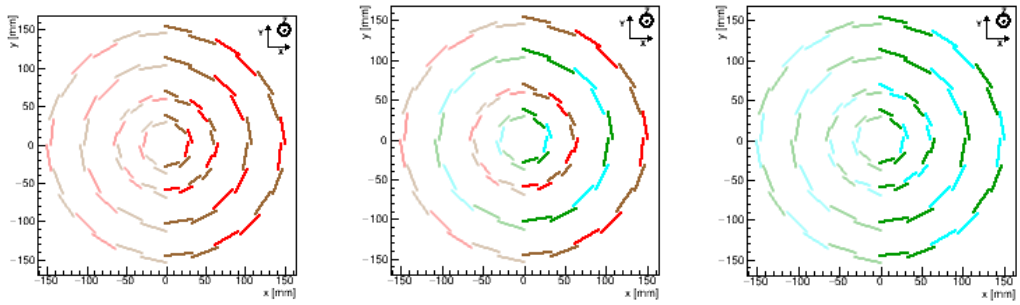


Figure 8. Serial power chains for TBPX short (top) and long (bottom) end. Every SP chain runs along two consecutive ladders: each layer needs #ladders/2 chains to get powered.

TFPX- TEPX

TFPX Even side of Dee TFPX Odd side of Dee

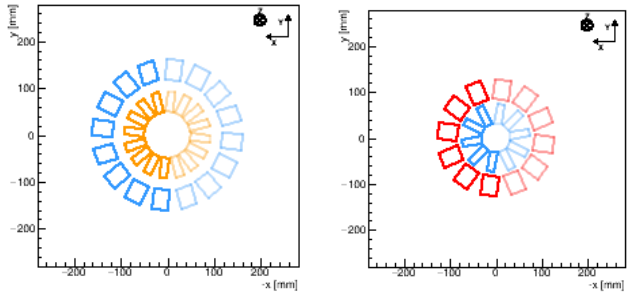


Figure 9. Serial powering of TFPX dees.

TEPX Odd side of Dee TEPX Even side of Dee

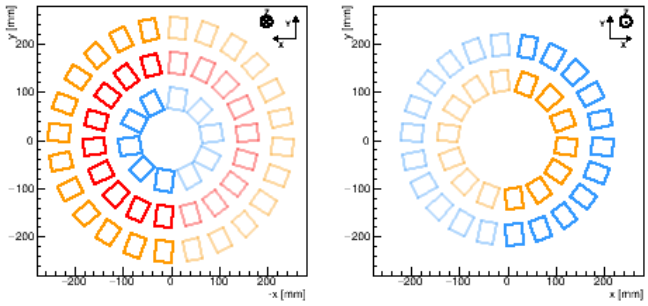


Figure 10. Serial powering of TEPX dees.

HIGH VOLTAGE DISTRIBUTION

Two HV lines are considered for the TBPX chains and one HV line per SP chain is currently the baseline for chains on the disks (TFPX,TEPX). Figure 12 shows that although the number of modules served by one HV line in the outer rings of TFPX and TEPX is significantly larger than the barrel ones (max 12 over max 5) their coverage is much smaller.

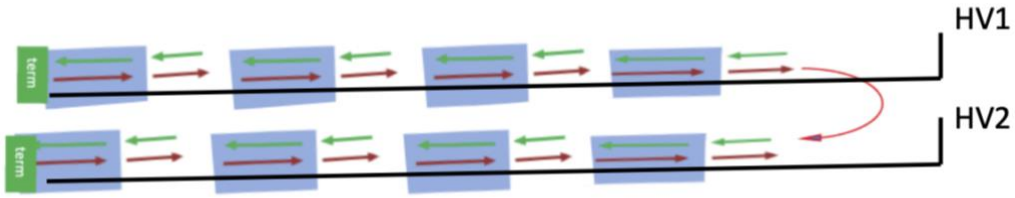


Figure 11 High Voltage distribution in the barrel. One SP chain will be served by two independent HV lines (no return line for HV, each HV line will serve a ladder).

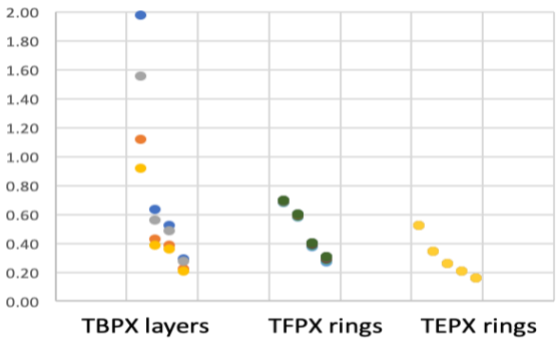


Figure 12. Δη Δφ coverage of HV groups.

Table 2. Summary of SP chains and HV lines needed to power the IT.

		SP Chains 1x2 modules	SP Chains 2x2 modules	SP Chains SUM	Number of modules per SP chain Z+	Number of modules per SP chain Z+	Number of HV lines
TBPX	L1 3D	3		3	10	8	6
	L2 3D	6		6	8	10	12
	L3		5	5	10	8	10
	L4		7	7	8	10	14
	SUM	**9**	**12**	**21**			**42**
TFPX	R1 3D	1		**1**	5		1
	R2	1		**1**	8		1
	R3		1	**1**	6		1
	R4		1	**1**	8		1
	Odd side of dee	1	1	2			2
	Even side of dee	1	1	2			2
	Dee	2	2	4			4
	Double Dee	4	4	8			
	SUM	**32**	**32**	**64**			**64**
TEPX	R1		1	**1**	5		1
	R2		1	**1**	7		1
	R3		1	**1**	9		1
	R4		1	**1**	11		1
	R5		1	**1**	12		1
	Odd side of dee		3	3			3
	Even side of dee		2	2			2
	Dee		5	**5**			5
	Double Dee		10	**10**			10
	SUM		**40**	**40**			**40**
QUARTER OF TBPX+TFPX		**41**	**44**	**85**			**106**
QUARTER OF TEPX			**40**	**40**			**40**
QUARTER OF IT		**41**	**84**	**125**			**146**
ONE END OF IT		**82**	**168**	**250**			**292**
ENTIRE IT		**164**	**336**	**500**			**584**

READOUT

E-LINKS

Triggered event data collected from the pixel array will be collected by the end of column of the pixel chip where pixel array data will get re-organized by on-chip data processing and are sent out after a lossless data compression algorithm has been applied. Chip data are sent over a configurable (1-4) number of differential electrical links (E-links) at 1.28 Gbps to the opto-modules that accommodate the LpGBT chip that converts the readout data to optical. Data from up to seven E-links are merged into 10 Gbps upstream optical links to the DAQ. Every module will also receive command, trigger and configuration data via a downstream 160 Mbps E-link originating from the LpGBT, which receives the data via a 2.5 Gbps downstream optical link. The number of E-links used to readout a chip depends on the location on the detector since there is a strong dependence on hit rates vs location. For outer pixel layers and rings, where the hit rates are low, the data from all the chips of the module are merged into a single E-link that comes out of the module. Notice also that for the disks, because of the $1/r^2$ dependence, the rate across a module is not uniform. The rates among disks of the same part of the detector are similar (small Z dependence). The current chip data formatting will include a binary tree logic that allows a reduction of the output bandwidth by a factor of x1.5-2.

Table 3. Date Rates before and after on-chip data compression per chip per event. (have not been updated recently, to be updated)

Pixel Size					Adding fixed AUR.overhead (4.59%)
25x100					
Region	Raw data size	Formatted size	Reduction	Bandwidth (Gbps)	Bandwidth (Gbps)
L1InnerCenter	6900	3581	1.93	2.69	2.81
L1InnerEnd	6698	3310	2.02	2.48	2.60
L2	1509	808	1.87	0.61	0.63
L3	703	373	1.88	0.28	0.29
L4 (center)	469	246	1.91	0.18	0.19
TFPXRing1Inner	2969	2014	1.47	1.51	1.58
TFPXRing1Outer	1578	1055	1.50	0.79	0.83
TFPXRing2Inner	1616	1092	1.48	0.82	0.86
TFPXRing2Outer	1015	672	1.51	0.50	0.53
TFPXRing3	734	472	1.56	0.35	0.37
TFPXRing4	494	306	1.61	0.23	0.24
TEPXRing1 Inner TBC	1237	**850**	1.45	0.64	0.67
TEPXRing1 Outer TBC	848	**583**	1.45	0.44	0.46
TEPXRing2	580	390	1.49	0.29	0.31
TEPXRing3	432	284	1.52	0.21	0.22
TEPXRing4	333	210	1.58	0.16	0.17
TEPXRing5	279	175	1.59	0.13	0.14
Pixel Size					Adding fixed AUR.overhead (4.59%)
50x50					
Region	Raw data size	Formatted size	Reduction	Bandwidth (Gbps)	Bandwidth (Gbps)
L1InnerCenter	7284	3664	1.99	2.75	2.87
L1InnerEnd	9007	3673	2.45	2.75	2.88
L2	1952	1033	1.89	0.78	0.81
L3	788	458	1.72	0.34	0.36
L4	469	283	1.66	0.21	0.22
TFPXRing1Inner	2670	1951	1.37	1.46	1.53
TFPXRing1Outer	1424	1022	1.39	0.77	0.80
TFPXRing2Inner	1469	1059	1.39	0.79	0.83
TFPXRing2Outer	914	643	1.42	0.48	0.50
TFPXRing3	675	461	1.46	0.35	0.36
TFPXRing4	434	286	1.52	0.21	0.22
TEPXRing1 Inner TBC	1067	**800**	1.33	0.60	0.63
TEPXRing1 Outer TBC	667	**500**	1.33	0.38	0.39
TEPXRing2	504	368	1.37	0.28	0.29
TEPXRing3	379	271	1.40	0.20	0.21
TEPXRing4	281	197	1.43	0.15	0.15
TEPXRing5	250	173	1.45	0.13	0.14

Table 4. Estimated number of E-links per subdetector part and E-links bandwidth occupancy. (have not been updated recently, to be updated)

Pixel Size		Adding fixed AUR.overhead (4.59%)	
25x100			
Region	Nlink	Bandwidth (Gbps)	Link Occ.(%)
L1InnerCenter	3	2.81	**73.15**
L1InnerEnd	3	2.60	**67.62**
L2	1	0.63	49.50
L3	0.5	0.29	45.78
L4 (center)	0.25	0.19	**60.34**
TFPXRing1Inner	2	1.58	61.71
TFPXRing1Outer	1	0.83	64.63
TFPXRing2Inner	1	0.86	66.92
TFPXRing2Outer	1	0.53	41.20
TFPXRing3	0.5	0.37	57.81
TFPXRing4	0.25	0.24	75.05
TEPXRing1 Inner TBC	1	0.67	52.09
TEPXRing1 Outer TBC	0.5	0.46	71.46
TEPXRing2	0.5	0.31	47.78
TEPXRing3	0.25	0.22	69.58
TEPXRing4	0.25	0.17	51.57
TEPXRing5	0.25	0.14	**42.94**
Pixel Size		Adding fixed AUR.overhead (4.59%)	
50x50			
Region	Nlink	Bandwidth (Gbps)	Link Occ.(%)
L1InnerCenter	3	2.87	**74.86**
L1InnerEnd	3	2.88	**75.04**
L2	1	0.81	63.33
L3	0.5	0.36	56.09
L4	0.25	0.22	69.39
TFPXRing1Inner	2	1.53	59.77
TFPXRing1Outer	1	0.80	62.63
TFPXRing2Inner	1	0.83	64.92
TFPXRing2Outer	1	0.50	39.40
TFPXRing3	0.5	0.36	56.52
TFPXRing4	0.25	0.22	70.16
TEPXRing1 Inner TBC	1	0.63	49.03
TEPXRing1 Outer TBC	0.5	0.39	61.28
TEPXRing2	0.5	0.29	45.14
TEPXRing3	0.25	0.21	66.46
TEPXRing4	0.25	0.15	48.35
TEPXRing5	0.25	0.14	42.40

Table 5. Estimated bandwidth in Mpbs per subdetector part. (have not been updated recently, to be updated)

QUARTER		Multiplicity (#ladders, #disks)	#modules/ladder		Bandwidth per module	Number of modules		Total Bandwidth [Gbps]	
			Z+	**Z-**		**Z+**	**Z-**	**Z+**	**Z-**
BARREL									
TBPX	**L1**	6	5	4	5.62	30	24	168.6	134.88
	L2	12	4	5	1.26	48	60	60.48	75.6
	L3	10	5	4	1.17	50	40	58.5	46.8
	L4	14	4	5	0.77	56	70	43.12	53.9
	4 layers SUM					184	194	330.7	311.18
DISKS			#modules/half disk						
TFPX	**R1**	8	10		2.41	80		192.8	
	R2	8	16		1.38	128		176.64	
	R3	8	12		1.48	96		142.08	
	R4	8	16		0.96	128		122.88	
	Odd dee		22			176		334.88	
	Even dee		32			256		299.52	
	1/2 disk		54						
	8 1/2 disks SUM					432		634.4	
TEPX	**R1**	4	10		2.24	40		89.6	
	R2	4	14		1.22	56		68.32	
	R3	4	18		0.84	72		60.48	
	R4	4	22		0.66	88		58.08	
	R5	4	24		0.55	96		52.8	
	Front side		52			208		202.88	
	Back side		36			144		126.4	
	Dee								
	1/2 disk		88						
	4 1/2 disks SUM					352		329.28	
QUARTER OF TBPX+TFPX						616	626	965.1	945.58
QUARTER OF TEPX						352		329.28	
QUARTER OF IT						968	978	1294.38	1274.86
ONE END OF IT						1936	1956	2588.76	2549.72
ENTIRE IT						3892		5138.48	

Table 6 Summary of number of links needed per subdetector part.

		Multiplicity (#ladders, #disks)	#modules per ladder/ ring		Data Links per module	Total Data Links		Control Links per module	Total Control Links		Electrical Links per ladder/ring		Total Electrical Links	
			Z+	Z-		Z+	Z-		Z+	Z-	Z+	Z-	Z+	Z-
TBPX	L1	6	5	4	6	180	144	1	30	24	35	28	210	168
	L2	12	4	5	2	96	120	1	48	60	12	15	144	180
	L3	10	5	4	2	100	80	1	50	40	15	12	150	120
	L4	14	4	5	1	56	70	1	56	70	8	10	112	140
	SUM					**432**	**414**		**184**	**194**			**616**	**608**
TFPX	R1	16	5		3	240		1	80		20		320	
	R2	16	8		2	256		1	128		24		384	
	R3	16	6		2	192		1	96		18		288	
	R4	16	8		1	128		1	128		16		256	
	SUM					**816**			**432**				**1248**	
TEPX	R1	8	5		3	120		1	40				160	
	R2	8	7		2	112		1	56		21		168	
	R3	8	9		1	72		1	72		18		144	
	R4	8	11		1	88		1	88		22		176	
	R5	8	12		1	96		1	96		24		192	
	SUM					**488**			**352**				**840**	
	Quarter of TBPX+TFPX					**1248**	**1230**		**616**	**626**			**1864**	**1856**
	Quarter of TEPX					**488**			**352**				**840**	
	Quarter of IT					**1736**	**1718**		**968**	**978**			**2704**	**2696**
	One end of IT					**3472**	**3436**		**1936**	**1956**			**5408**	**5392**
	Entire IT					**6908**			**3892**				**10800**	

LPGBTS

The conversion of the readout data to optical links at 10 Gbps by LpGBTs and the Versatile Links (VL+) is constrained to a maximum total dose 100 Mrad and to a fluence of 3 x 10^{15} n_{eq}/ cm^2, accounting the fluence from neutrons>20MeV with a factor of x1 and the fluence from charged hadrons>20MeV with a factor of x2 (based on private communication with Jan Troska). Therefore, the LpGBT modules will be located at the periphery of the dee structures named cartridges. One replacement of the portcards has been foressen for the portcards.

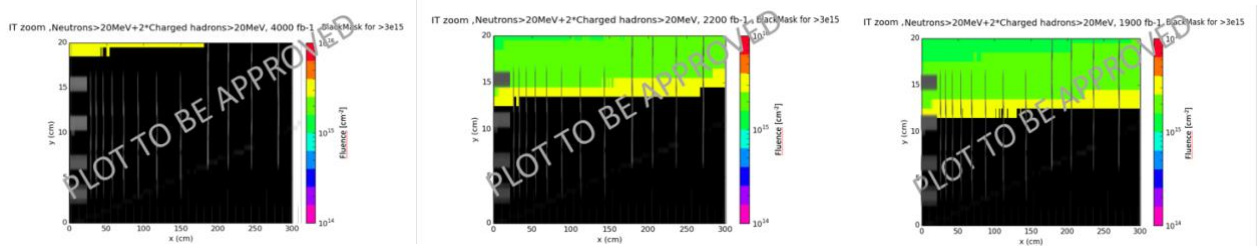


Figure 13. The above maps are showing the total fluence expected after 4000fb-1, 2200 fb-1 and 1900 fb-1 (from left to right). The black areas correspond to an "excluded" area because of the rad levels. (plots to be approved by BRIL radsim team).

E-links originating from nearby chips and modules can be arriving in the same LpGBT (up to 7 inputs). The constraints of the elinks to LpGBTs grouping are the following:

- Max inputs of LpGBT is 7
- All links of a module connects to the same LpGBT (cannot split modules in multiple LpGBTs)
- A LpGBT can be shared amongst modules that belong to the same power chain.
- No front-to-back connection is allowed for the E-links.

Below Figures 14-16 show how these rules apply for the detector parts. The number in each cell corresponds to the E-links per module. Each cell corresponds to a module. Each row corresponds to a ladder. Each rectangular frame shows a group of links readout by a LpGBT (done only for one SP as an example for barrel). Each yellow line is a SP chain. Figure 17 is an illustration of the groups of the total number of LpGBTs needed for each part of the detector for a quarter of IT.

		max modules per LpGBT	#modules per SP chain		#LpGBTs Used per SP chain		#Portcards per SP chain	
			Z+	Z-	Z+	Z-	Z+	Z-
TBPX	L1	1	10	8	10	8	4	3
	L2	3	8	10	3	4	1	2
	L3	3	10	8	4	3	2	1
	L4	7	8	10	2	2	1	1
	SUM							
TFPX	R1	2	5		3		1	
	R2	3	8		3		1	
	R3	3	6		2		1	
	R4	7	8		2		1	
	SUM							
TEPX	R1	2	5		3		1	
	R2	3	7		3		1	
	R3	7	9		2		1	
	R4	7	11		2		1	
	R5	7	12		2		1	

TBPX MODULES TO LPGBTS

TBPX L1 TBPX L2 TBPX L3 TBPX L4

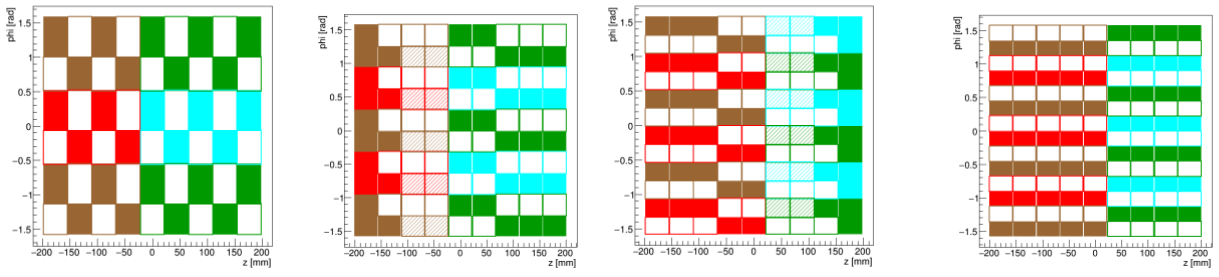


Figure 14. LpGBTs needed per TBPX Serial Power chain for the short and long end of the barrel layers. 1 color <=> 1 serial power chain. Within each serial power chain: different fills (contour or full) to distinguish different GBTs.

DEES (TFPX- TEPX)

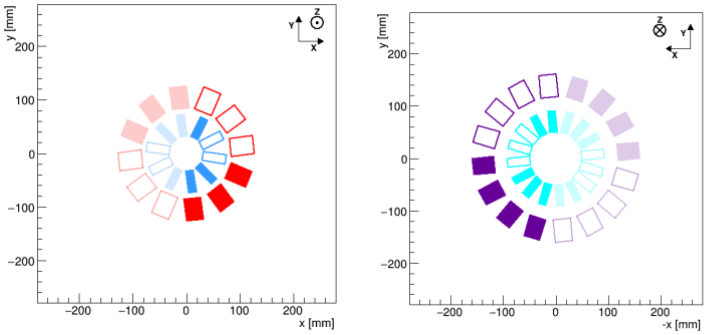


Figure 15. LpGBTs needed per TFPX Serial Power chain. 1 color <=> 1 serial power chain. Within each serial power chain: different fills (contour or full) to distinguish different GBTs.

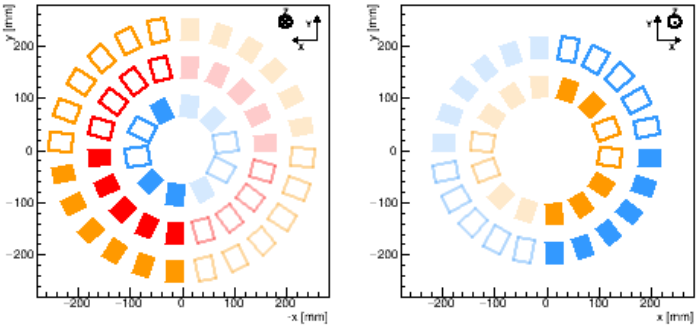
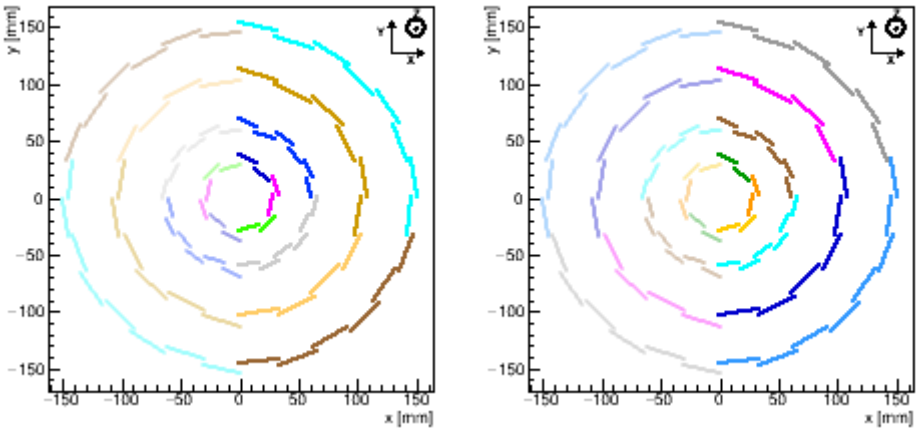


Figure 16. LpGBTs needed per TEPX Serial Power chain. 1 color <=> 1 serial power chain. Within each serial power chain: different fills (contour or full) to distinguish different GBTs.

TBPX Z- and Z+, TFPX, TEPX



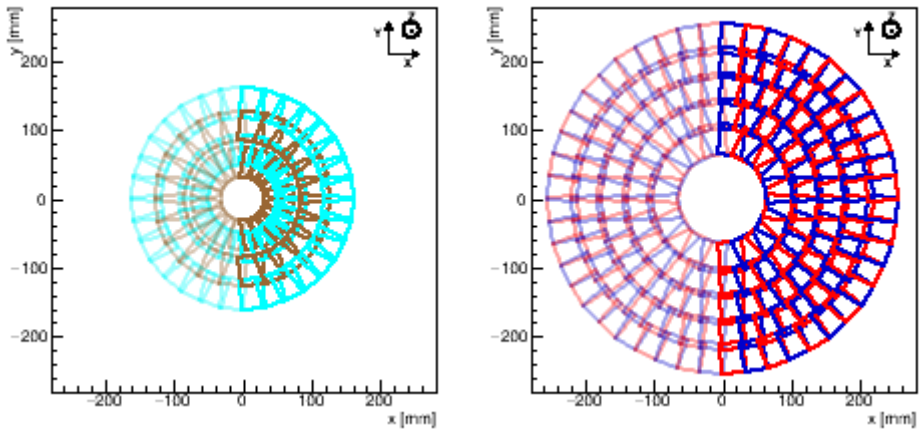


Figure 17. A map of the groups of the LpGBTs needed for each part of the IT for a quarter of the detector. For each (X) half: 1 color <=> 1 MFB.

MULTIFIBRE BUNDLES

At Patch Panel 0 (PP0) the fibers originating from nearby LpGBTs will be grouped together in multi-fiber bundles of 24 fibers (MFB). The grouping of the LpGBT links to multi-fiber bundles follows the constraints:

- One MFB serves 12 LpGBTs (24 fibers, 12 upstream-12 downstream).
- One MFB should serve LpGBT that are sitting close to each other (following similar routing).
- No mixing of TEPX services with the TFPX-TBPX allowed.

The following summary Table 7 uses the information presented in Table 6 and Figure 17 and presents how the LpGBT links can be grouped in bundles of 12 pairs and the percentage of fibers used in the bundles.

Table 7 Summary table for #GBTs/MFBs per sub-detector

		Portcards/SPchain		Portcards		LpGBTs/ SPchain		LpGBTs		MFBs only used VTRx+	
		Z+	Z-	Z+	Z-	Z+	Z-	Z+	Z-	Z+	Z-
	L1	4	3	12	9	10	8	30	24	3	3
	L2	1	2	6	12	3	4	18	24	2	2
TBPX	L3	2	1	10	5	4	3	20	15	2	2
	L4	1	1	7	7	2	2	14	14	2	2
	SUM			**35**	**33**			**82**	**77**	**9**	**9**
	R1	1		1		3		3			
	R2	1		1		3		3			
	R3	1		1		2		2			
	R4	1		1		2		2			
TFPX	Odd side			2				5			
	Even side			2				5			
	Dee			4				10		1	
	DoubleDee			8				20		2	
	SUM			**64**				**160**		**16**	
	R1	1		1		3		3			
	R2	1		1		3		3			
	R3	1		1		2		2			
	R4	1		1		2		2			
	R5	1		1		2		2			
	Front Face			3				7			
	Back Face			2				5			
TEPX	**One dee**			**5**				**12**		1	
	DoubleDee			**10**				**24**		2	
	SUM			**40**				**96**		**9***	EXTRA MFB for D4R1bril
Quarter of TBPX+TFPX				**99**	**97**			**242**	**237**	**25**	**25**
Quarter of TEPX				**40**				**96**		**9**	
Quarter of IT				**139**	**137**			**338**	**333**	**34***	**34***
Entire IT				**552**				**1342**		**136**	

*the 9th MFB dedicated to BRIL is not accounted in the tklayout cabling page.

MULTIFIBRE CABLES

At Patch Panel 1 (PP1) multi-fibre bundles will be grouped together to multi-fibre cables (MFC) (144 fibres each). Grouping the MFBs here was done keeping in mind that it would be nice to mix data from the TBPX layers and the TFPX disk such that a DTC failure would not cause complete loss a big part of the detector.

- One MFC serves 6 MFBs (72 GBTs).
- Each MFC will be serving one DAQ module with 72 inputs.
- One MFC can combine different regions.
- The services for TEPX are completely separated by the rest of the IT.

The following summary table shows the grouping of the MFBs to MFC and the respective input bandwidth for a DTC module. The 6 MFBs will be served by 1 MFCs, hence 1 DTC. The rest of the 25 MFBs for TBPX and TFPX can be served by 5 DTCs/MFCs.

Table 8. Mapping of the multifibre bundles to multifibre cables and DAQ modules.

DTC	Reading out	MFB
#1	L1	3
#2	L2+ 1 TFPX dd	4
#3	L3+ 2 TFPX dd	6
#4	L4+ 2 TFPX dd	6
#5	3 TFPX dd	6
#6	2 TEPX dd	4
#7	2 TEPX dd	4
BRIL TDC	TEPX D4R1	1