CMS Tracker PLL Reference Manual

P. Placidi, A. Marchioro and P. Moreira

CERN - EP/MIC, Geneva Switzerland

July 2000

Version 2.0

Chapter1

Introduction

The CMS Tracker PLL (**TPLL**) is a custom IC that was designed for *clock* and *trigger* distribution in the CMS central tracker. This document provides a functional and physical description of the TPLL ASIC from the user perspective.

CLOCK AND TRIGGER DISTRIBUTION

In the CMS central tracker system, the LHC reference clock (40.08MHz) and the first level trigger decisions (L1) are transmitted from the counting room to the detector using a single optical fibre. To achieve this, both the clock and the first level trigger signals are encoded as a single signal as is schematically illustrated in Figure 1. The encoding is done so that whenever the trigger system issues a first level trigger reject decision, the coded signal is identical to the LHC clock signal. However, when an accept decision is issued by the central trigger processor, the coded signal simply stays at logic level “0” for the duration of a LHC clock cycle.

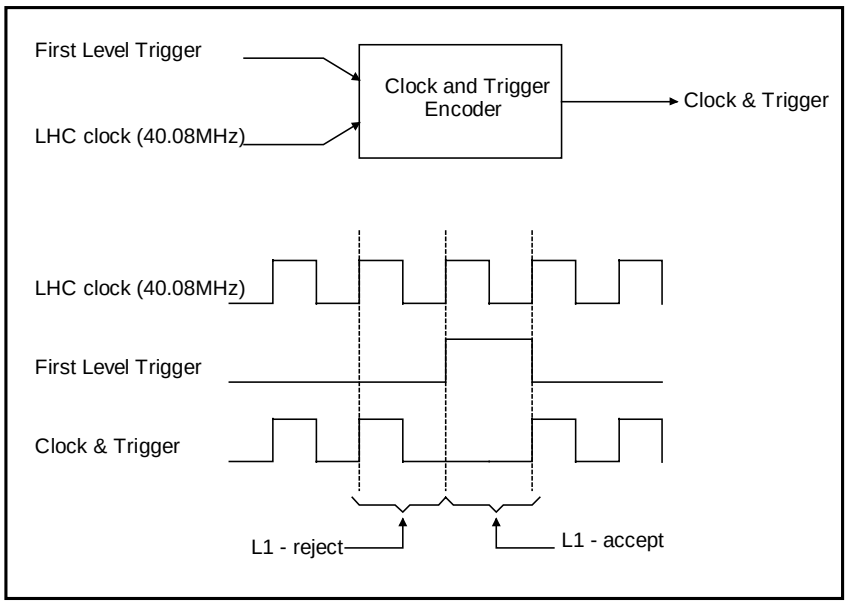

Figure 1 Combined coding of the LHC clock and first level trigger signals

This conceptually simple scheme allows to reduce the number of physical channels necessary to transmit the clock and the trigger information to the detectors. However, at the receiving end, a special purpose circuit is required to extract from the encoded signal the original information. The Tracker PLL ASIC (TPLL) implements this function: it extracts the LHC clock from the encoded signal and decodes the first level trigger decisions. An important function of any clock and trigger distribution network is the ability to correct the timing of the clock and trigger signals according to the geographical positioning of the different subsystems inside the detector. This function is also implemented by the TPLL. The ASIC contains an internal clock de-skewing mechanism that allows to phase shift the clock signal up to a maximum of 25ns in

phase steps of 1.04ns. A trigger coarse skew compensation function is also implemented that allows to delay the L1 trigger signal up to a maximum of 15 LHC clock cycles.

ASIC architecture

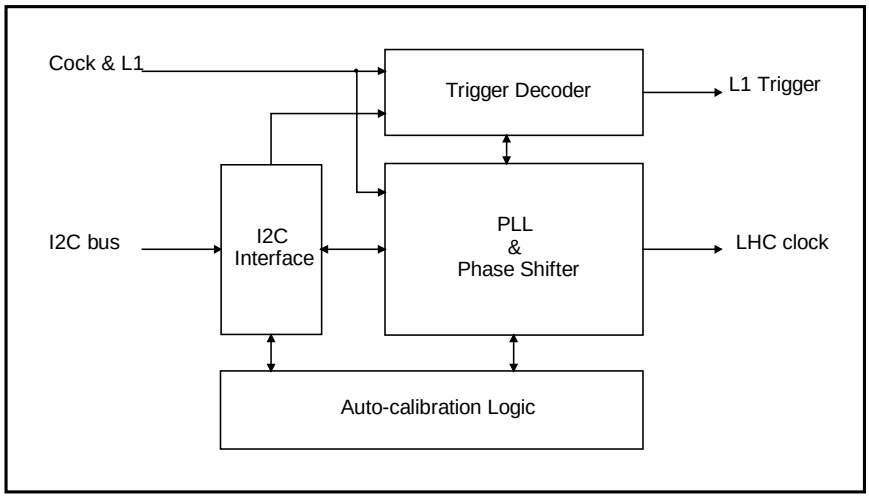

Figure 2 CMS Tracker PLL architecture

The basic architecture of the TPLL is shown in Figure 2. The ASIC is essentially composed of the following functional elements: the Trigger Decoder logic, the PLL & Phase Shifter, the I2C Interface and the Auto-Calibration logic.

As discussed before, combining the clock and the L1 trigger information requires extra circuitry in the system to extract from the encoded signal the original information, that is, the LHC 40.08MHz clock and the first level trigger decisions L1. These are, respectively, the functions of the PLL and of the Trigger Decoder logic. Besides clock recovering, the PLL circuit also implements the clock Phase Shifter. This function is implemented by a VCO composed of 12 delay cells that generate 12 different clock phases evenly distributed between zero and half LHC clock period (T_{LHC} = 24.95ns). By selecting one of these clock phases, it is possible to phase shift the output clock signal between 0ns and $T_{LHC}/2$. Clock phases between $T_{LHC}/2$ and T_{LHC} are covered by inversion of the 12 internal VCO clock signals. Selection of the output clock phase is done by the user through the I2C interface.

For protection against Single Event Upsets (SEU) due to radiation, the IC logic is protected by triple voting. The I2C interface gives the user the possibility to check for the occurrence of an SEU. Since the redundancy scheme used in the IC does not automatically correct the register(s) in error, the user will have to reprogram the IC in order to prevent that multiple errors will lead to an error condition. A bit in the Control/Status register reports that if at least one SEU error was detected by the triple redundancy logic.

Finally, the ASIC contains an Auto-Calibration logic element that sets the PLL optimum bias conditions at start-up. The auto-calibration mechanism is transparent to the user. However, it can be controlled by the I2C interface for testing purposes.

The IC operation is controlled by a set of five registers that can be written and read using the I2C serial interface. These registers are:

- Control and Status Register 1 (CTR1)
- Control and Status Register 2 (CTR2)
- DAC Low Control Register (CTR3)

- DAC High Control Register (CTR4)
- L1 Trigger Delay Control Register (CTR5)

The detailed operation of these registers will be described in the following chapters.

Chapter 2

I2C Register Addressing

All the internal registers are accessible through the I2C interface for read and write operations. The I2C addressing of the internal registers is discussed in this chapter.

I2C INTERFACE

I2C data transactions to and from the TPLL ASIC are done on a byte basis, that is, each I2C cycle addresses a single 8-bit register in the IC. The ASIC and its registers are identified by a seven-bit address. Of the seven address bits, the two least significant bits (I2CA1 and I2CA0) are used to select one of the internal registers while the five most significant bits (I2CA6 to I2CA2) represent the ASIC I2C address. The IC I2C address is defined by five pins named I2CA6 to I2CA2, which must be hardwired to set a valid address.

Internally the chip contains five registers with the following corresponding addresses:

Control and Status Register 1 (CTR1):	I2CA<1:0> = 0
Control and Status Register 2 (CTR2):	I2CA<1:0> = 1
DAC Low Control Register (CTR3):	I2CA<1:0> = 2
DAC High Control Register (CTR4):	I2CA<1:0> = 3 (& CTR2<5> = 0)
L1 Trigger Delay Control Register (CTR5):	I2CA<1:0> = 3 (& CTR2<5> = 1)

Notice that CTR4 and CTR5 share the same I2C address, I2CA<1:0> = 3. Distinction between the two registers is made by bit 5 of the Control and Status Register 2. It is thus necessary to set the desired value in CTR1<5> before accessing registers CTR4 or CTR5.

Chapter 3

Registers

The Tracker PLL IC contains five internal registers that control the ASIC operation. The functionality of these registers is described in this chapter.

TRACKER PLL IC REGISTERS

Control and Status Register 1 (CTR1)

This register allows the user to change the TPLL operation mode between normal and test mode.

After a reset, the normal operation mode is set by default (CTR1<7>=0). In this case, the auto-calibration logic drives the lock acquisition process. After a reset sequence bit CTR1<0> (“Going”) can be monitored to check for the successful completion of the auto calibration cycle.

The ASIC can be set in the test mode by forcing bit CTR1<7> to 1. In this case, the I2C interface can be used to gain full control of the PLL. When the test mode is set, the four registers CTR1, CTR2, CTR3 and CTR4 have direct control of the PLL operation overriding the auto-calibration logic.

Another important function of this register is that it allows the ASIC to be reset via the I2C interface. For this, the user should write a one-zero sequence to bit CTR1<3>. Bit CTR1<3> also reports the SEU status of the ASIC when read back.

The full functionality of this register is described in the table below.

Bit	Name	Function	RST State
7	Mode	0 – Normal mode: the PLL operation is controlled by the auto calibration circuit. 1 – Test mode: the PLL operation is controlled by the I2C interface. In this case, the calibration multiplexer is forced to use the contents of register CTR3 and CTR4 to select the bias current of the VCO. Bits <7:6> of CTR2 become active.	0
6	DisableT1	0 – trigger outputs (T1A and T1B) enabled 1 – trigger outputs disabled	0
5,4	TestSelect<1:0>	These two bits select the signal that is observed on the trigger outputs (T1A and T1B) when they are enabled (CTR1<6>=0): 00 – trigger signal active (normal operation) 01 – phase detector ~up signal 10 – phase detector ~down signal	00

		11 – PLL comparator output: "0" → V(filter) < V(reference) "1" → V(filter) > V(reference)	
3	Restart/SEU	Write operation: a "1" to "0" write sequence in this bit resets the PLL. Read operation: this bit reports the SEU status of the IC: "0" – no SEU detected "1" – at least one SEU detected	0
2	ForcePFD	Forces the phase frequency detector to be used. This bit is enabled when CTR1<7>=1	0 (after phase lock)
1	HighGain	This is a read only bit. It reports the status of the HighGain signal of the auto-calibration state machine: "0" – low loop gain "1" – high loop gain	-
0	Going	This is a read only bit. This bit should be "1" after a normal reset sequence	1 (after phase lock)

Table 1 Control and Status Register 1 (CTR1) bit assignments

Control and Status Register 2 (CTR2)

Under normal operation this register main use is to program the clock phase and to select between registers CTR4 and CTR5 when the ASIC is addressed with internal address bits I2CA<1:0> = 11.

If the test mode is active, bits CTR2<7> and CTR2<6> are used to directly control the PLL operation.

The output clock phase is selected by bits CTR2<4> and CTR2<3:0>. To program clock phases between 0 and $T_{LHC}/2$, bit CTR2<4> must be set to zero. In this case the clock phase will be given by CTR2<3:0> $\times$ 1.04ns, where CTR2<3:0> can be any of the numbers: 1,2 … 11 (decimal). Clock phases between $T_{LHC}/2$ and T_{LHC} are obtained by setting CTR2<4> to one. In this case, the phase is given by: $T_{LHC}/2$ + CTR2<3:0> $\times$ 1.04ns.

Bit	Name	Function	RST State
7	I2C_Going	If in test mode (CTR1<7>=1), writing a one to this bit forces the signal "Going" to be active independently from the state of the auto-calibration state machine.	0
6	I2C_HighGain	If in test mode (CTR1<7>=1): 0 – PLL low loop gain 1 – PLL high loop gain	0
5	RSEL	0 – selects CTR4 at internal address 3 1 – selects CTR5 at internal address 3	0

4	PhaseInvert	0 – for clock phases between 0 and $T_{LHC}/2$ 1 – for clock phases between $T_{LHC}/2$ and T_{LHC}	0
3:0	Phase<3:0>	This is a number between 0 and 11 (decimal) that allows to phase shift the clock signal in time steps of 1.04ns	0

Table 2 Control and Status Register 2 (CTR2) bit assignments

DAC Control Registers (CTR3 and CTR4):

These two 8-bit registers contain together a 16-bit value used set the VCO bias current. In the normal operation mode (CTR1<7>=0), the value set in these registers by the auto-calibration logic is read back by an I2C read operation. When in the test mode (CTR1<7>=1), the result of the previous I2C write operations to these registers is read back.

Register CTR4 is accessed only if the internal address I2CA<1:0> = 3 is received and bit CTR2<5> is set to zero.

Bit	Name	Function	RST State
7:0	DACL<7:0>	VCO bias control word low byte	0

Table 3 DAC Low Control Register (CTR3)

Bit	Name	Function	RST State
7:0	DACH<7:0>	VCO bias control word high byte	0

Table 4 DAC High Control Register (CTR4). (I2CA<1:0> = 3 & CTR2<5>=0)

L1 Trigger Delay Control Register (CTR5)

In this register, the trigger signal delay is programmed. This delay is measured in multiples of the LHC clock cycle (T_{LHC}) and can have take any of the values 0,1, …, 15 (decimal).

Register CTR5 is accessed only if the internal address I2CA<1:0> = 3 is received and bit CTR2<5> is set to one.

Bit	Name	Function	RST State
<3:0>	L1Delay<3:0>	Trigger delay in multiples of LHC clock cycles	-

Chapter 4

TPLL Basic User Operations

Under normal conditions, only a few basic operations will be required from the part of the user to guaranty the correct operation of the ASIC. This chapter reviews the basic procedures that will be executed by the user during normal operation (this excludes any test mode procedures).

ASIC RESET

There are two means to reset the ASIC. These include an external reset signal (hardware reset) and a software reset which is executed by writing a one-zero sequence in bit CTR1<3> of the Configuration and Status Register 1. This starts an auto-calibration and lock acquisition cycle. All the registers are returned to their default values after reset.

STATUS MONITORING

Status monitoring of the IC is done by reading the Control and Status Register 1. Of this register, two bits are of special interest: CTR1<3> and CTR1<0>. Bit CTR1<0> reports the successful (CTR1<0>=1) or unsuccessful (CTR1<0>=0) completion of an auto-calibration cycle after reset.

The ASIC logic is implemented using a triple voting mechanism to increase the circuit robustness against single event upsets. When an SEU is detected by the triple voting logic, bit CTR1<3> of the Control and Status Register 1 is set to “one” to warn that at least an error was detected. Notice that the triple voting mechanism used is not self-correcting and, consequently, multiple errors in the same signal will eventually lead to erroneous operation of the ASIC. Consequently, each TPLL ASIC in the tracker system should be monitored at regular intervals and reinitialised in the case of an SEU error being detected. The periodicity of the checks and the concrete action to be taken is still under discussion.

SELECTING THE CLOCK PHASE

The clock phase is programmed using bits CTR2<4> and CTR2<3:0> of the Control and Status Register 2. By setting bit CTR2<4> to zero the user chooses clock phases between 0 and $T_{LHC}/2 - \Delta_{step}$ where T_{LHC} = 24.95ns is the LHC clock period and Δ_{step} = 1.04ns is the minimum phase step that can be programmed. If bit CTR2<4> is set to one, the possible clock phases are between $T_{LHC}/2$ and $T_{LHC} - \Delta_{step}$. The actual clock phase value is set by bits CTR2<3:0> and given by CTR2<3:0> $\times$ 1.04ns if CTR2<4>=0 or by $T_{LHC}/2$ + CTR2<3:0> $\times$ 1.04ns if CTR2<4>=1. Bits CTR2<3:0> can take any of the values: 1, 2, …, 11 (decimal).

SELECTING THE TRIGGER DELAY

The trigger delay is programmed by writing a number between 0 and 15 (decimal) in the L1 Trigger Delay Control Register (CTR5). The trigger signal can be delayed between 0 and 15 LHC clock cycles. To access this register the user must first write a “one” to bit CTR2<5> in the Control and Status Register 2 and then use the internal address 3 (I2CA<1:0> = 3).

During selection of register CTR5, care must be exercised not to disturb the contents of the clock phase settings (CTR2<4:0>) when writing bit CTR2<5> in the Control and Status Register 2.

Chapter 5

IC Pins and Packaging

In this chapter, the IC signals, layout and package are discussed

IC EXTERNAL SIGNALS

CLKIN, ~CLKIN – reference signal input, LVDS levels

CLKA, ~CLKA – LHC clock output pins, LVDS levels

CLKB, ~CLKB – LHC clock output pins, LVDS levels

GND – 0V power pins

I2CA2 to I2CA6 – I2C address inputs, CMOS levels

~Reset – Reset input, active low, CMOS levels

SCL – I2C clock input, CMOS levels

SDA – I2C serial data input/output pin, CMOS levels input, open drain output

T1A, ~T1A – Trigger output, LVDS levels

T1B, ~T1B – Trigger output, LVDS levels

VDD – 2.5V power pins

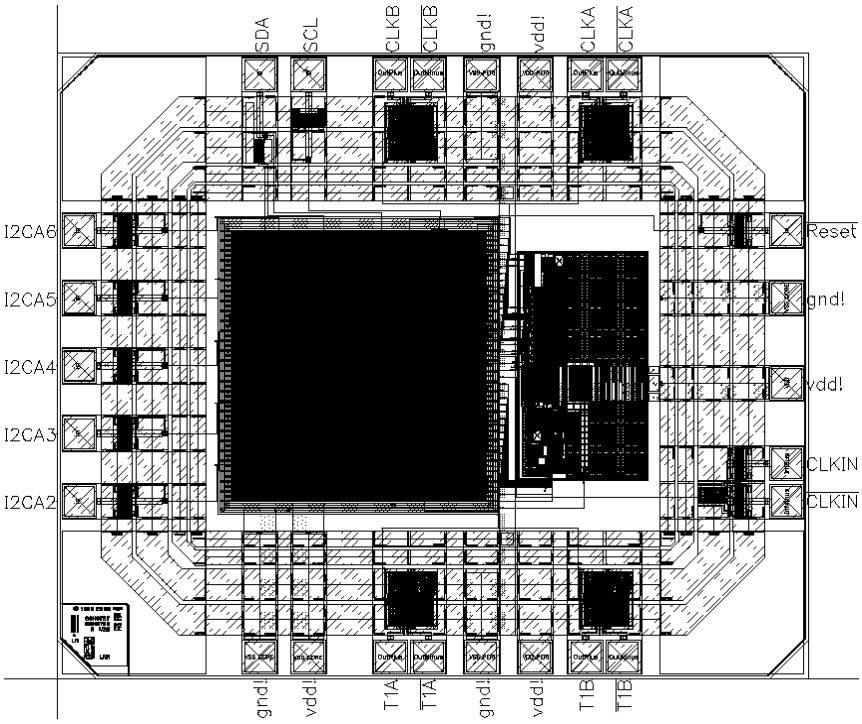

Figure 3 Trigger PLL ASIC layout

PACKAGE

To be defined!