

LCDS Driver Chip

Functions:

1) fan-out of LCDS control signals to modules:

CLK, CTR, SDA

with adjustable delays. The delay is set by applying Logical high or low at the input A0 (LSB) to A3 (MSB).
(The pads have internal pull-down resistors)

$$D = 0.235 \text{ ns} * (2^3 A3 + 2^2 A2 + 2^1 A1 + A0)$$

all bits high = longest delay

all bits low = shortest delay

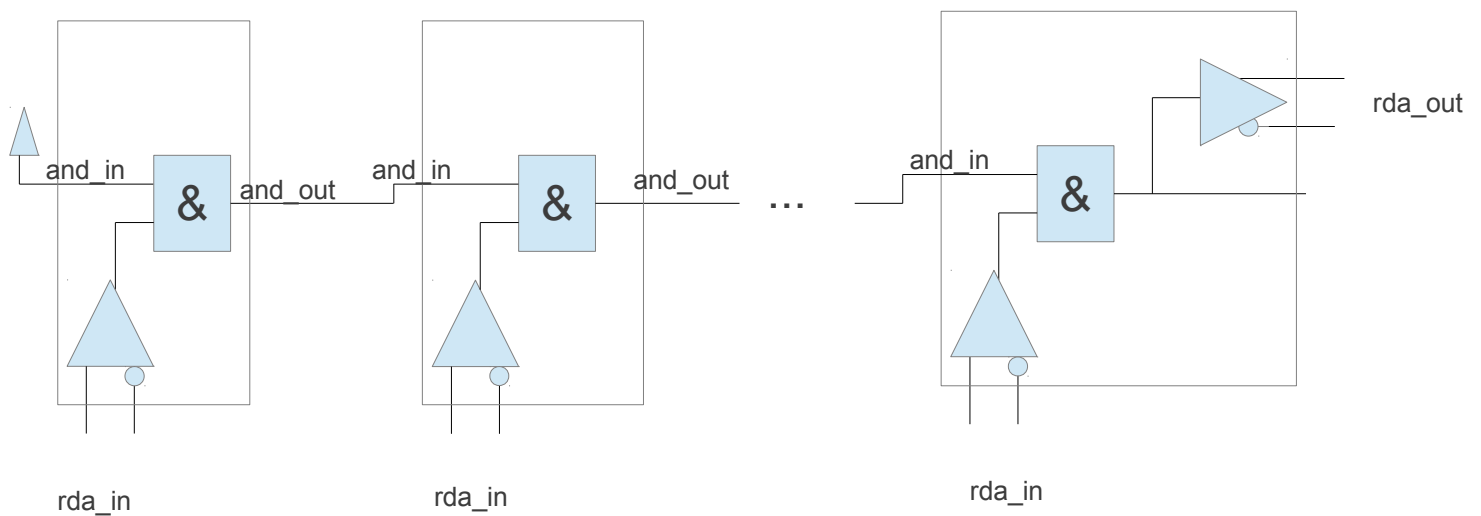
2) fan in for LCDS return signals RDA. The LCDS chips Form a chain, and each LCDS driver makes the logical AND (not NAND) of

a) RDA from one module (LCDS)

b) RDA from the previous LCD driver (CMOS)

The result is available as a CMOS level (to be fed into the following chip in the chain) and differential LCDS (only used for the last chip in the chain).

3) fan out for the hard-reset (not used for phase 1 modules))



Notes:

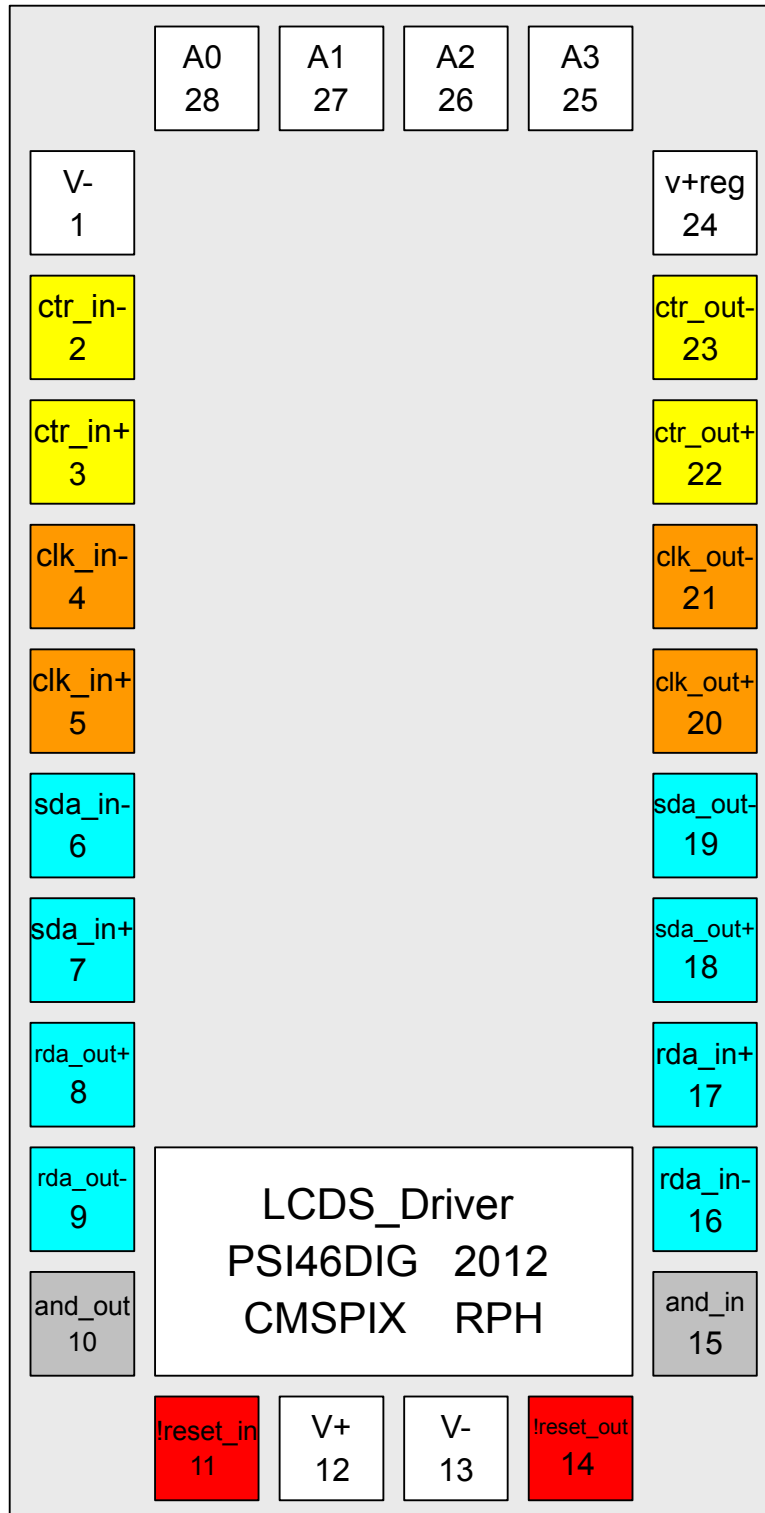
1) The RDA output of a TBM is high when it is idle. All TBMs connected to the chain are controlled by the same SDA but should have different Hub addresses, such that only one TBM is returning data at any given time.

2) Layer 1 HDIs have two RDA output which should always return exactly the same data. Only one of them will be connected to the LCDS Driver.

3) The RDA inputs have built-in termination resistors (value ??) to gnd. Other LCDS inputs are not terminated.

4) Older versions of this Driver should not be used because of a mistake in the AND chain logic.

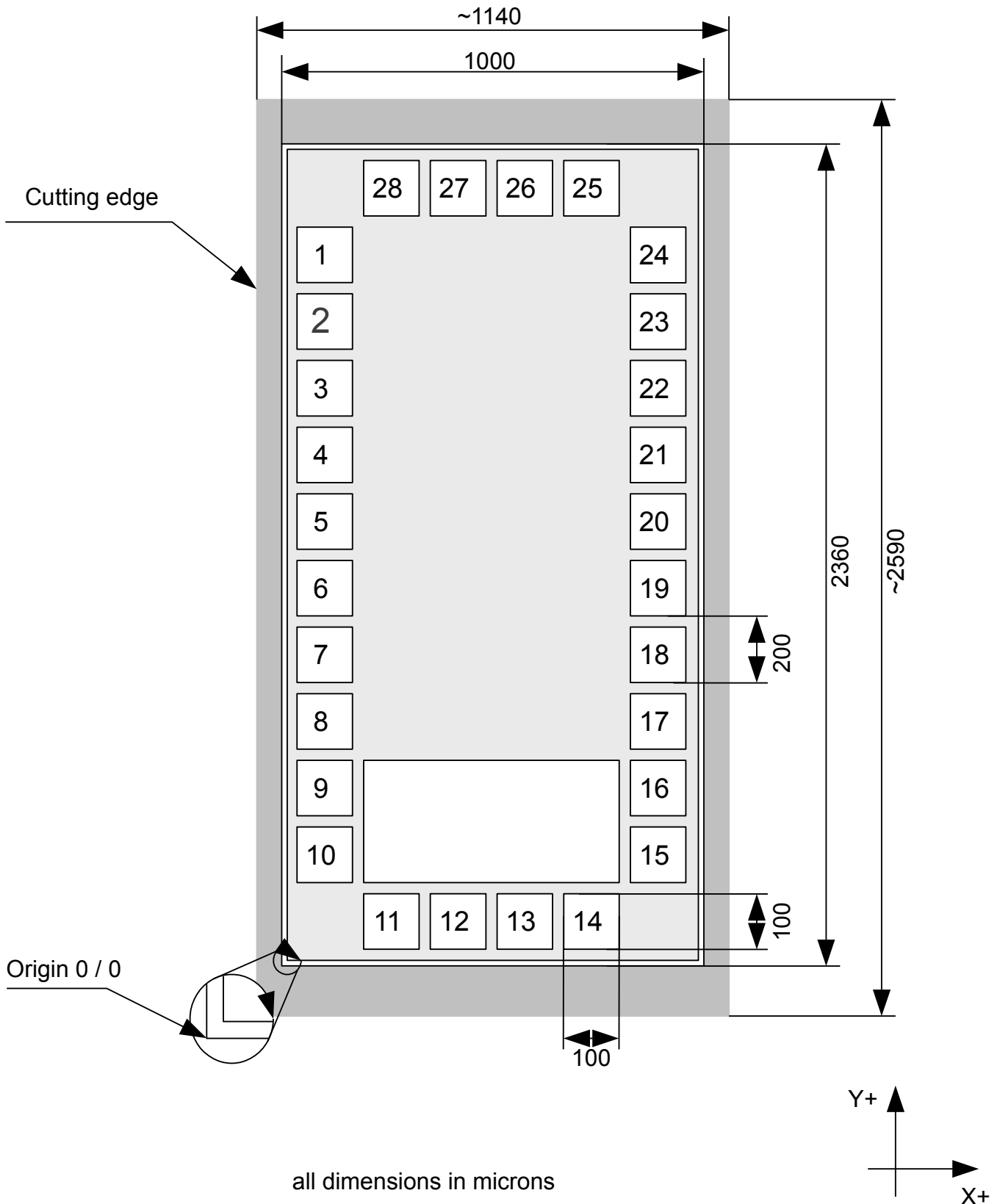
LCDS Driver



Die size: 1000um x 2360um **Die Thickness:**
180um **Wirebond Pads:** 28

PSI / CMS Pixel Barrel

LCDS Driver Die dimensions



all dimensions in microns

any drawing on this sheet is not true to scale

last modified 05.07.2013

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