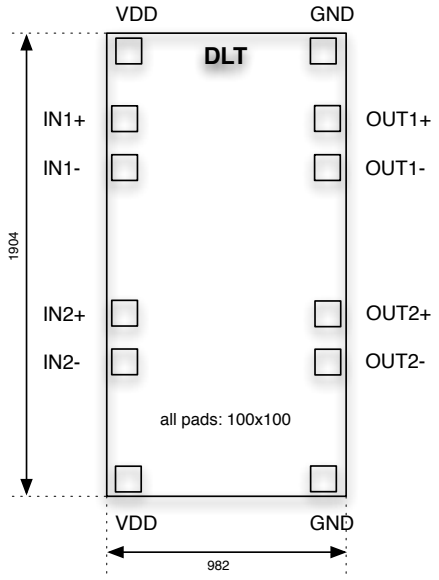
Digital Level Translator (DLT)

Chip Layout



Pin Description

Signal	*Description*
GND	Power Ground
VDD	Power +2.5 V to Ground
IN1+/IN1-	Differential Input of Level Translator (Channel 1)
IN2+/IN2-	Differential Input of Level Translator (Channel 2)
OUT1+/OUT1-	Differential Voltage Output (Channel 1)
OUT2+/OUT2-	Differential Voltage Output (Channel 2)

Electrical Specifications

There are four different versions of the DLT chip. All DLT versions were designed for a working resistance of $R = 100\ \Omega$. However, other values of R can be used to choose the desired output swing.
Common parameters to all versions are

Parameter	*Typ*	*Unit*
Supply Voltage VDD	2.5	V
Output Common Mode Voltage	0.5	VDD
Working Resistance	100	Ω

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DLT

- Simplest design.
- Common Mode not stable after input signal change

  $\Rightarrow$ However corrected by internal regulation circuit.

Parameter	*Simulated Value*
Total Supply Current	5.8 mA/channel
Output Swing	CM $\pm$ 200 mV

DLT Tx

- Modified driver stage to stablize output common mode.

Parameter	*Simulated Value*
Total Supply Current	6.0 mA/channel
Output Swing	CM $\pm$ 200 mV

DLT Pw

- Enlarged output swing
- Improved timing between falling / raising edge

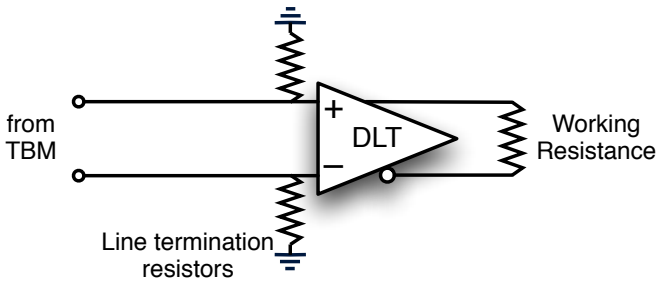
Parameter	*Simulated Value*
Total Supply Current	11.9 mA/channel
Output Swing	CM $\pm$ 0.5 V

DLT RT

- Faster internal receiver.

Parameter	*Simulated Value*
Total Supply Current	13.5 mA/channel
Output Swing	CM $\pm$ 0.5 V

Typical Application Circuit



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