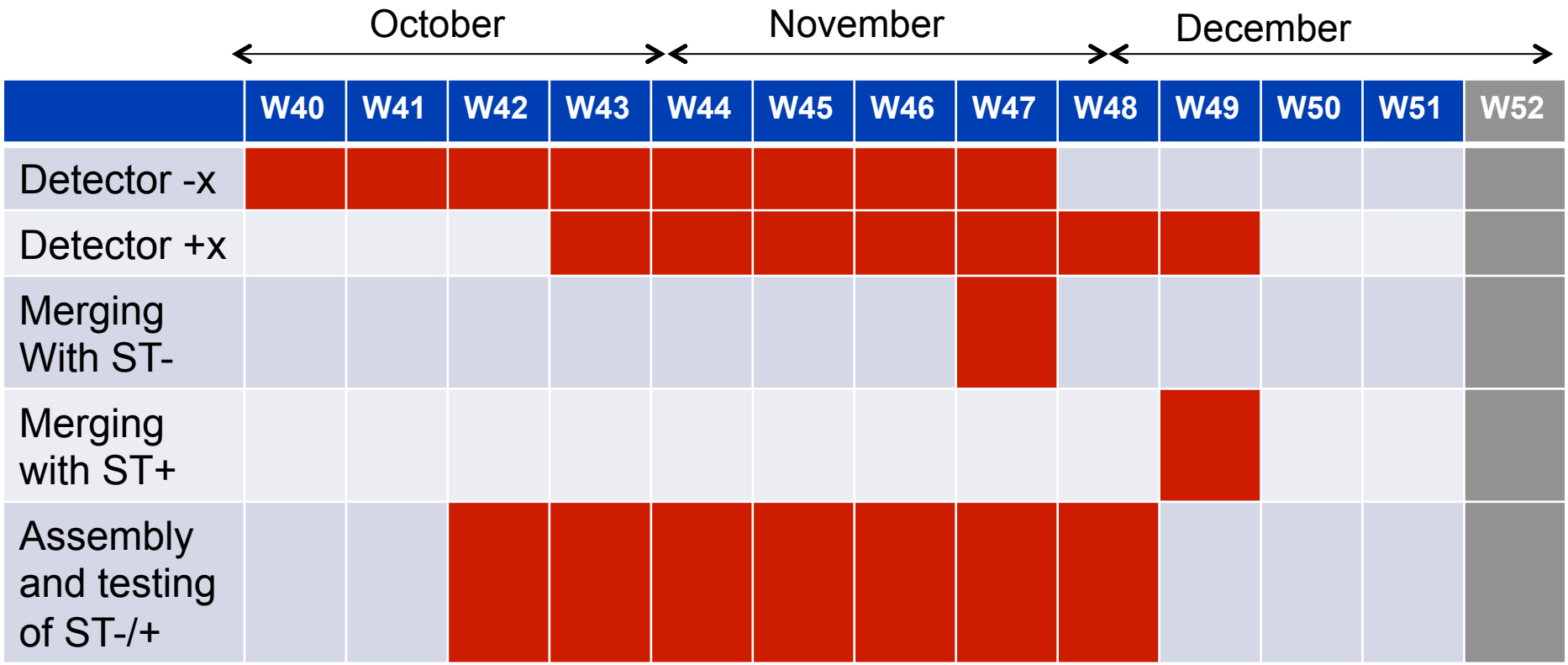
Towards assembly



Assembly: Peter, David, Lea
Testing: Riccardo, Yuta, Alberto, Lea, (Malte, Jen)

Assembly 1-2 days per quadrant
Testing involves functionality test (without cooling) and cold tests

Testing procedure (sector-by-sector)

Functionality test without cooling:

- Check LV and HV distribution (voltmeter)

BPixelTools and UZH testboard:

- CCU redundancy
- DCDC enabling/disabling
- I2c programming and resets
- POH bias scan
- SDA/RDA scan
- Data transmission test

Backup (in case of problems)

- Vana scan
- TBMPLL delay scan

Testing procedure (sector-by-sector)

Functionality test without cooling:

- Check LV and HV distribution (voltmeter) → Status of load test CB?

BPixelTools and UZH testboard:

- CCU redundancy
- DCDC enabling/disabling
- I2c programming and resets
- POH bias scan
- SDA/RDA scan → Configuration of scan region? Storage of results? Storage of settings?
- Trigger distribution → Storage of results? Storage of settings?
- Data transmission test → Treatment of not fully equipped POH bundles?

Backup (in case of problems)

- Vana scan
- TBMPLL delay scan

Testing procedure at cold

1) Passive test at cold (-20C)

2) DCDC load test for all sectors (sector-by-sector) at +17C

→ To be tested at system test

3) Functionality test of one sector per quadrant

- using VME POS → Status in the following slides
- run full sequence developed by Jen up to PixelAlive
- might be repeated at different temperatures (+17C, -20C)
- need configuration → Check which modules to use with Malte

Hardware

For now leave setup in lab untouched and build independent system at workshop:

- CAEN PS ready and tested → Lea: Bring MSC from PSI
- DAQ installed → Merge latest software updates, test at lab, move on digFED (check firmware)

- All electronic boards available
- Flex cables need to be bent → First, need to be checked, folding can be done quickly
- POHs: 133 out of 152 bundles built.
  Status of testing? → Can we finish this week?
- DOHs: bundles need to be assembled → Lea + … next week

- Connector board testing:
  - need to improve tooling for L4
  - 20 CB L12 to test. → Can this be done next week? Riccardo, Alberto?

POS commissioning sequence

- Start with configuration from module testing
- Delay25
- TBMPLL delay scan
- POH bias scan
- ROC delay scan
- VcthrCalDel
- TBMPLL delay scan for readback test
- Iana readback
- Idig readback
- PixelAlive
- BB test

Configuration:

- L1, L2 and L34 modules (using PSI46dig) implemented
- L1 modules with PROC600 still to be implemented

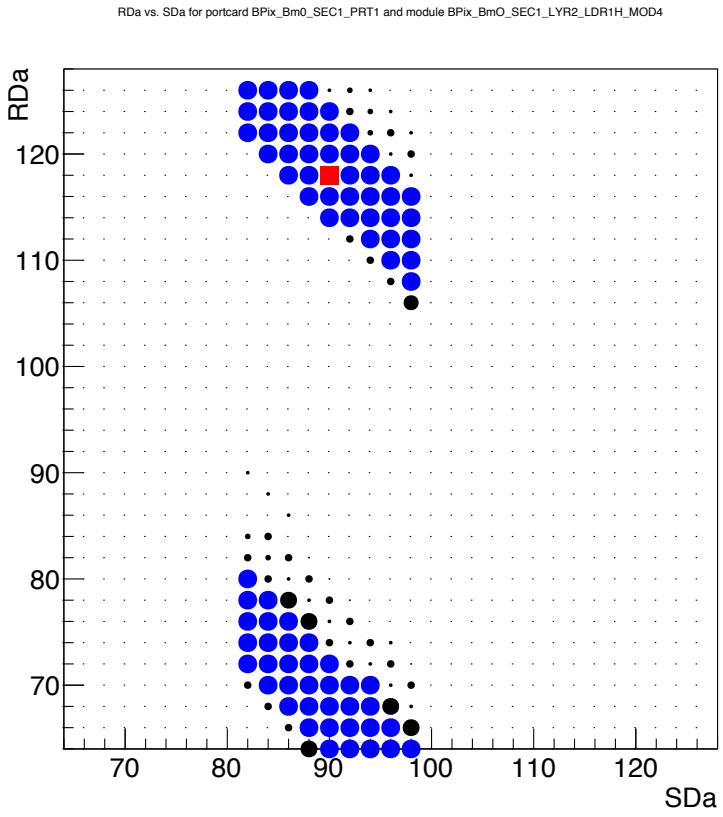
POS commissioning sequence

- Start with configuration from module testing → Need to add Iana/VD calibration (Pirmin)
- Delay25
- TBMPLL delay scan
- POH bias scan → Being implemented by Yuta
- ROC delay scan → Can we add reading of readback bit?
  → Do we need adjustment for L1?
- VcthrCalDel
- TBMPLL delay scan for readback test → Either separate or together with ROC delay
- Iana readback → Is file format for calibration data fixed?
- VD readback
- PixelAlive
- BB test → Pirmin

Configuration:

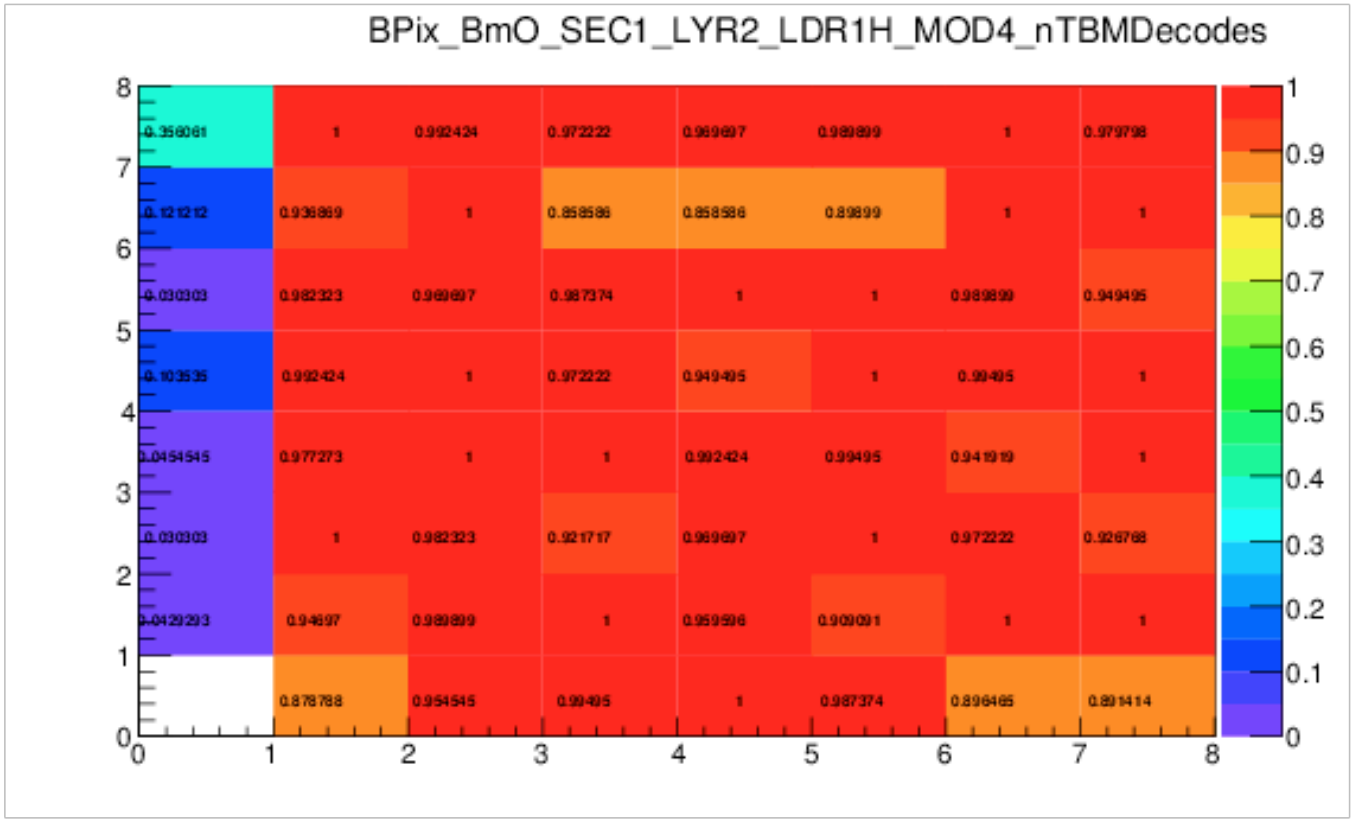
- L1, L2 and L34 modules (using PSI46dig) implemented
- L1 modules with PROC600 still to be implemented → Yuta

Delay25



- Verify: communication with TBM (CLK, SDA, RDA lines), hub addresses
- Status of calibration: Implemented and running

TBMPLLDelay

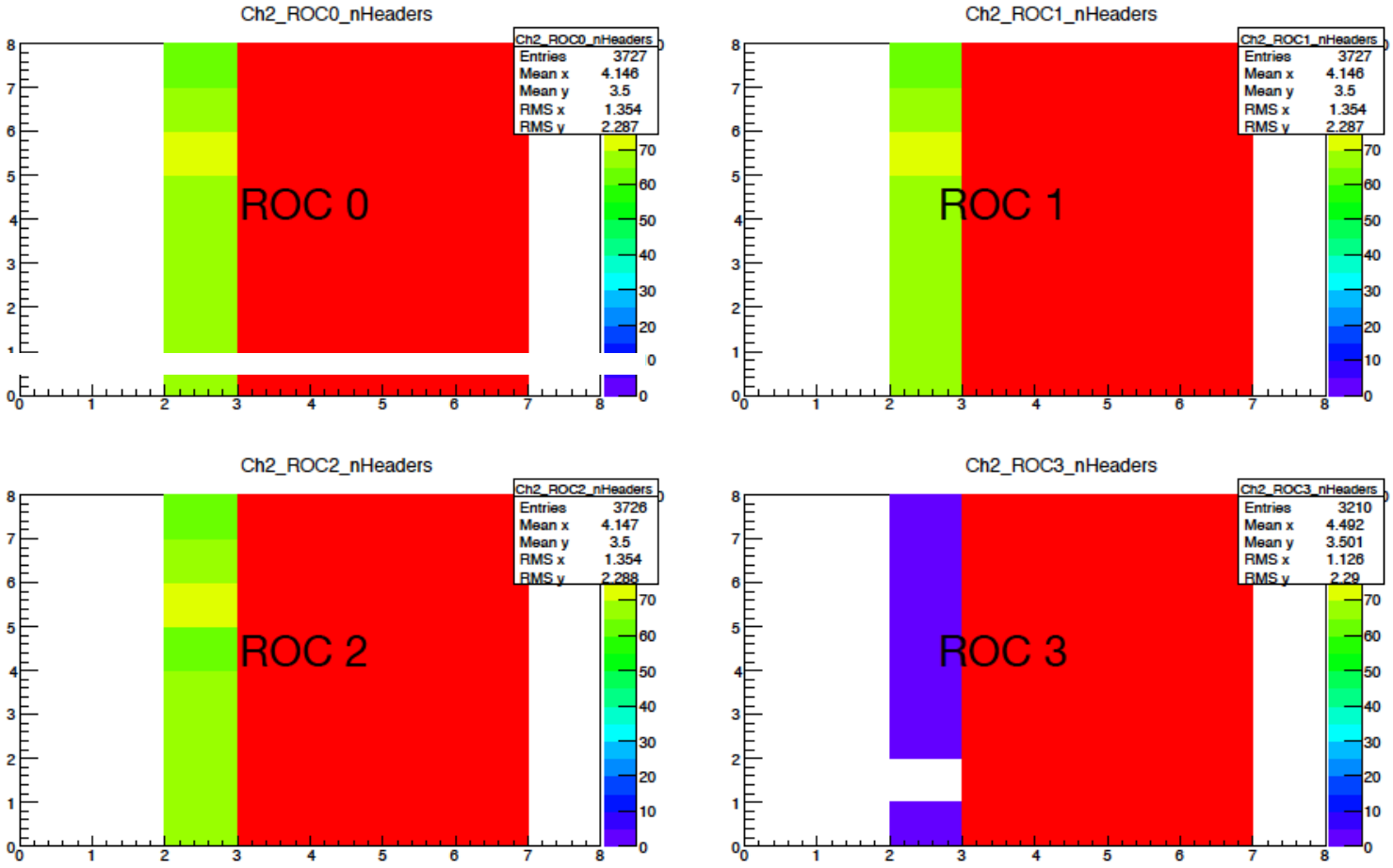


- Verify: Trigger distribution, TBM programming, readout
- Status of calibration: Implemented and running

POH bias scan

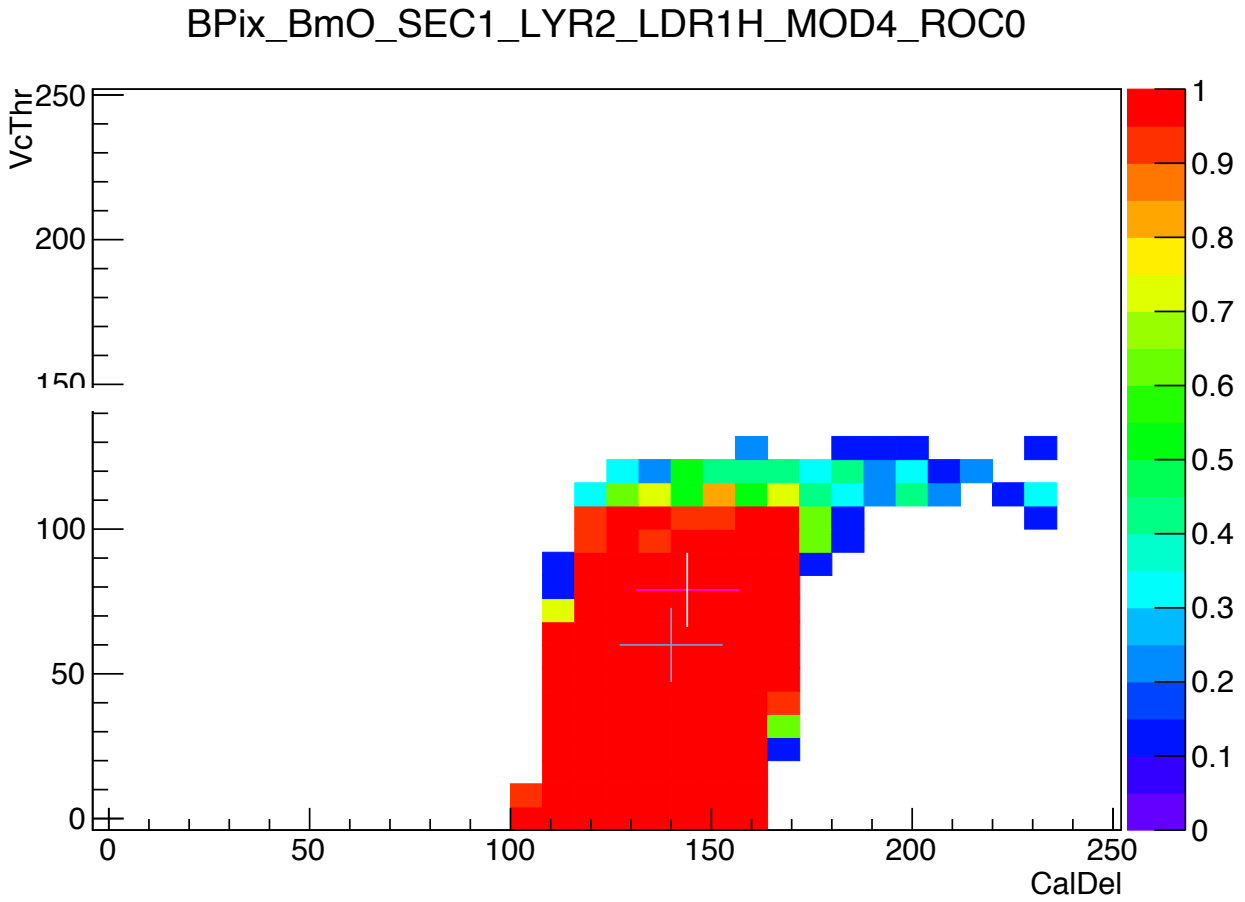
- Scan POH bias (and gain) and measure efficiency of decoding TBM H+T at each scan point
- Verify: Laser setting adjustment
- Status of calibration: Being implemented by Yuta

ROCDelay



- Verify: Token passage, number of ROCs per FED channel
- Status of calibration: Implemented and running

VcThrCalDel

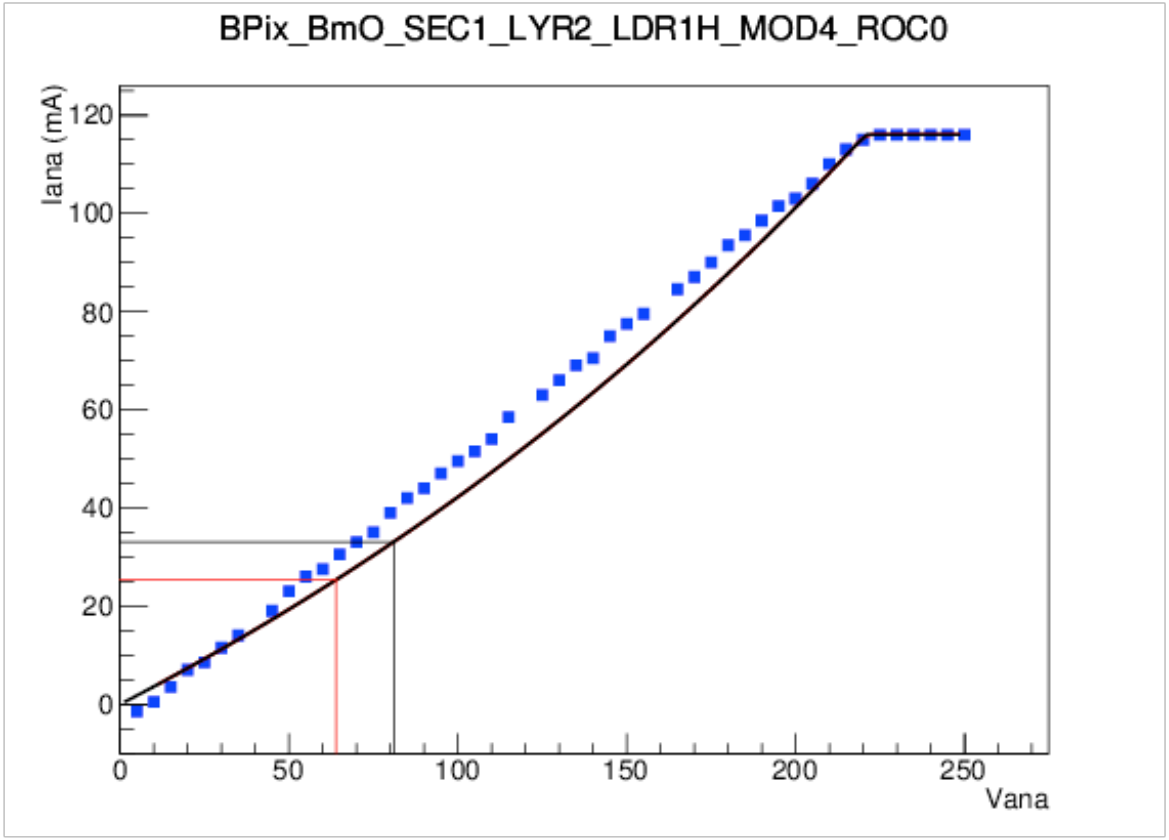


- Verify: ROC programming, CAL injection
- Status of calibration: Implemented and running
- (Is needed at this point already since proper functionality of readback data needs injection of hits for some ROCs)

TBMPLL adjustment for readback

- Scan TBMPLLDelay settings and readback ROC i2c addresses
- Verifies: TBMPLL delay settings, functionality of readback, assignment of ROCs and FED channels
- Status of calibration: Software to perform the calibration steps ready, still needs to be implemented as calibration

Iana readback



- Verify: ROC configuration
- Status of calibration: Implemented and running
- In addition: Vdig

PixelAlive

- Verify: Functionality of pixel
- Status of calibration: Implemented and running (PixelAlive 5x5)
- Use to test HV distribution to modules