Token Bit Manager 09 Chip Documentation

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I. Introduction

The Token Bit Manager (TBM) is an essential element of the front-end readout for the CMS pixel detector. It is a custom, mixed-mode, radiation-hard IC that controls and orchestrates the readout of a group of pixel ReadOut Chip (ROCs). The TBM is designed to be located on the detector near (< 15 cm.) to the pixel ROCs. The chip is intended to be mounted as a bare die, wire bonded to a printed circuit board, on the detector modules and will control the readout of 8 to 16 ROCs depending upon the barrel layer radius, or disk blade.

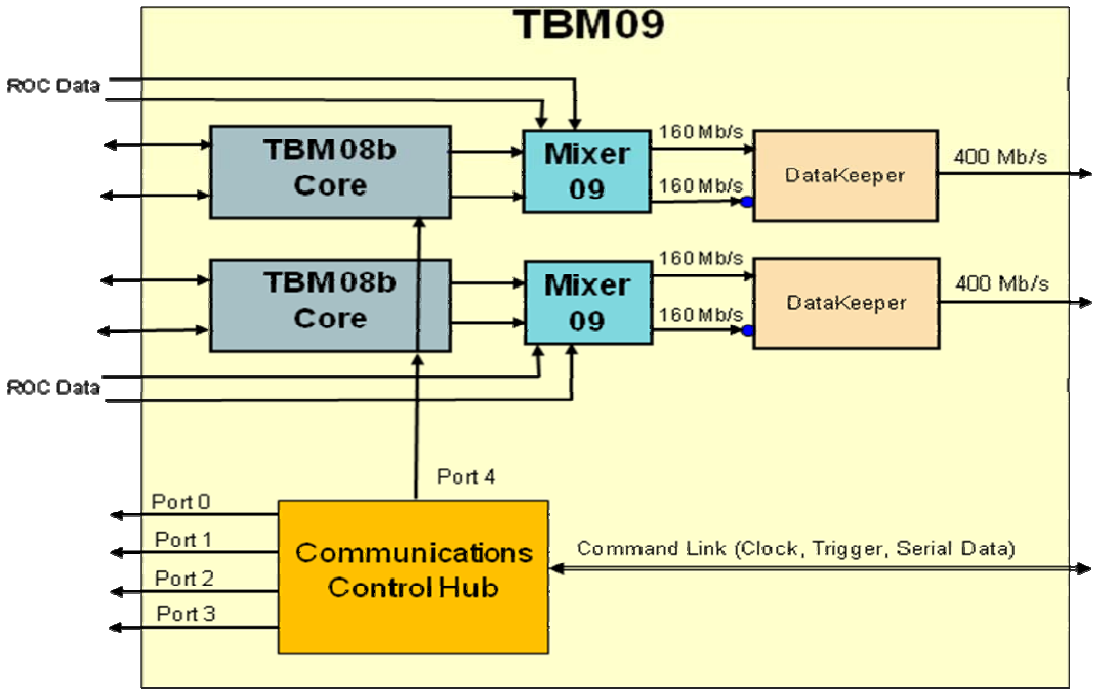


Figure 1: TBM09

A TBM 09 contains five major blocks as shown in Figure 1. These blocks consist of two TBM cores, two DataKeepers (multiplexor and encoder), and a Communications Control Hub.

II. TOKEN BIT MANAGER (CORE)

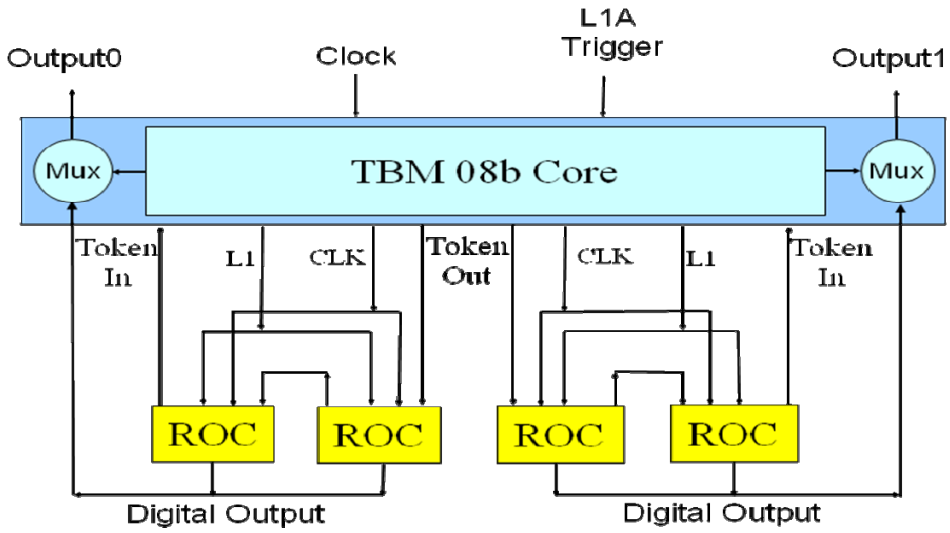


Figure 2: Schematic of a readout chain consisting of a TBM and a group of ROCs.

A TBM and the group of ROCs that it controls are connected to a mulitplexer/encoder block that will combine the two data streams. Then use a 4 to 5 bit encoder, to transmit the data at 400 Mb/s over an optical link, sent to the Front End Driver, located in the electronics house. The relationship of the TBM to the group of ROCs it controls is shown in Figure 2.

The principle functions of the TBM include the following.

- It will distribute the Level 1 triggers (L1A), and clock to the ROCs.
- Each arriving Level 1 trigger will be placed on a 32-deep stack awaiting its associated token pass. Normally the stack will be empty but is needed to accommodate high burst rates due to either noise, high track density events or trigger bursts. Note: Only the first 16 triggers placed on the stack will be passed to the ROCs, and have an associated token pass. All others will be marked in the trailer as a No Token Pass event (NTP). This is done to keep the DAQ synchronized, while speeding up the clearing of the STACK.
- It will control the readout of the ROCs by initiating a token pass for each incoming Level 1 trigger.
- On each token pass, it will write a header and a trailer word to the data stream.
- The header will contain an 8-bit event number. In a future revision, the unused 8 bit word will contain a temperature measurement.
- The trailer will contain 10-bits of error status. several error status bits, plus how many events are awaiting readout. This trailer will only be sent out, after the second of the two tokens are returned. Zeros will fill in on the shorter of the two readouts.

A TBM receives three control signals. A 40 MHz. clock, synchronized to the CMS beam crossing, a serial data line for configuration settings (discussed later) and an serial encoded trigger signal.

III. ELECTRICAL CHARACTERISTICS

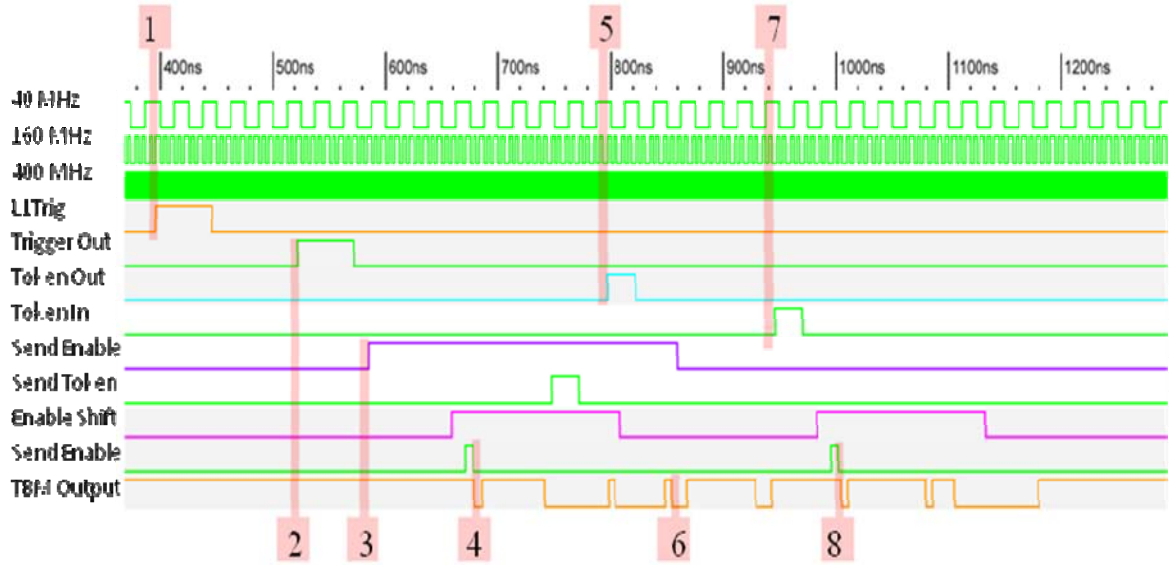
Supply Voltage (+Vd) +2.5 v

Power Consumption * 60 mW

(* With 4 Readout Chips Connected to Output Ports)

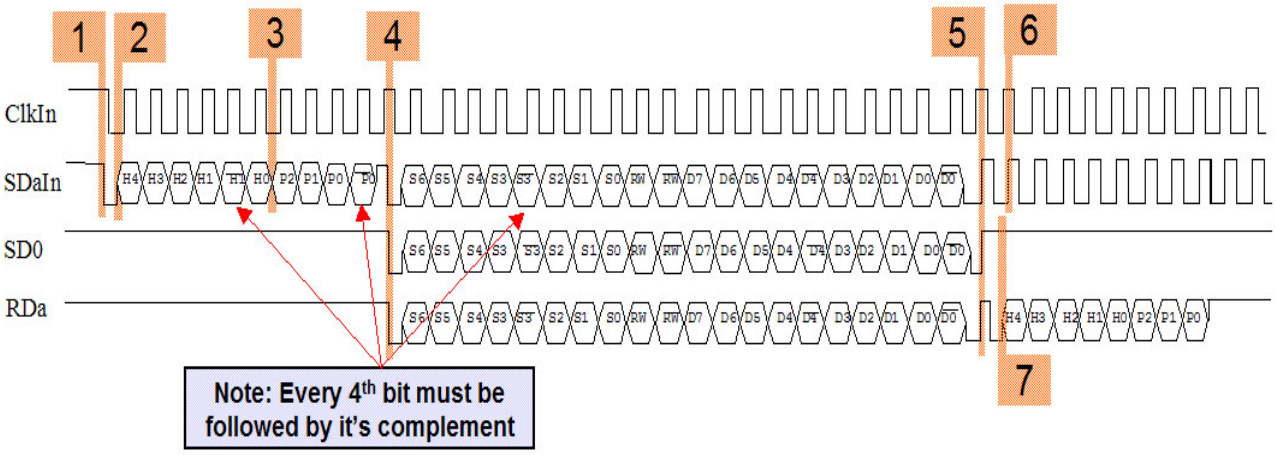
Pin #	Signal	Description
1	Termination	Termination for SDaIn/ClkIn/TrigIn: Gnd = 60Ω - Floating = 30Ω
3/2	+/- Tok Out 0	Token Output
5/4	+/- CK0	Clock Out to ROC, Port 0
7/6	+/- Tr0	Trigger Out to ROC, Port 0
9/8	+/- SDa0	Serial Data Out to ROC, Port 0
11/10	+/- Tok In 0	Token Input to switch from Serial In 0 to Serial In 1
13/12	+/- SerIn 0	Serial Data In From ROC, Port 0
15/14	+/- SerIn 1	Serial Data In From ROC, Port 1
17/16	+/- Tok In 1	Token Input to switch from Serial In 0 to Serial In 1
19/18	+/- SDa1	Serial Data Out to ROC, Port 1 From TBM A
21/20	+/- Tr1	Trigger Out to ROC, Port 1 From TBM A
23/22	+/- CK1	Clock Out to ROC, Port 1 From TBM A
24	Cap 1	Bypass Cap for LVDS low level
25,26, 40,41,65,66,81	GND	Power Supply Return
27,28, 38,39	VD+	Digital Power (+2.5 v) (27,28 - Periphery Power / 38,39 - Core/PLL Power)
30/29	+/- Tok In 1	Token Input to switch from Serial In 1 to Serial In 2
31	HA0	LSB of HUB Address
32	HA1	Second Bit of HUB Address
33	HA2	Third Bit of HUB Address
34	HA3	Forth Bit of HUB Address
35	HA4	MSB of HUB Address
37/36	+/- Tok Out 2	Token Output Repeats Signal from Token In 1
42	Cap 2	Bypass Cap for LVDS high level
44/43	+/- CK2	Clock Out to ROC, Port 2 From TBM B
46/45	+/- Tr2	Trigger Out to ROC, Port 2 From TBM B
48/47	+/- SDa2	Serial Data Out to ROC, Port 2 From TBM B
50/49	+/- Tok In 2	Token Input to switch from Serial In 2 to Serial In 3
52/51	+/- SerIn 2	Analog Data In From ROC, Port 2 To TBM B
54/53	+/- SerIn 3	Analog Data In From ROC, Port 3 To TBM B
56/55	+/- Tok Out 3	Token Output Repeats Signal from Token In 3
58/57	+/- SDa3	Serial Data Out to ROC, Port 3 From TBM B
60/59	+/- Tr3	Trigger Out to ROC, Port 3 From TBM B
62/61	+/- CK3	Clock Out to ROC, Port 3
64/63	+/- Tok In 3	Final Token Input, triggers sending trailer
68/67	+/- SerOutβ	Serial Data Output From TBM to FED
70/69	+/- ClkIn	System Clock Input
72/71	+/- TrigIn	Encoded Trigger Input
74/73	+/- SDaIn	Serial Command Data Input
76/75	+/- RDa	Serial Command Data returned to FEC
77	PCap	Bypass Cap for PLL Regulator
79/78	+/- SerOutα	Serial Data Output From TBM to FED
80	Dcap	Bypass Cap for Core Regulator

IV. SIGNAL TIMING



1) L1A Trigger Starts
2) L1A Trigger Output to ROC
3) Readout Process Begun
4) TBM Header Started
5) Token Sent to ROCs
6) Header Ends
7) Token Returned From Rocs
8) TBM Trailer Started

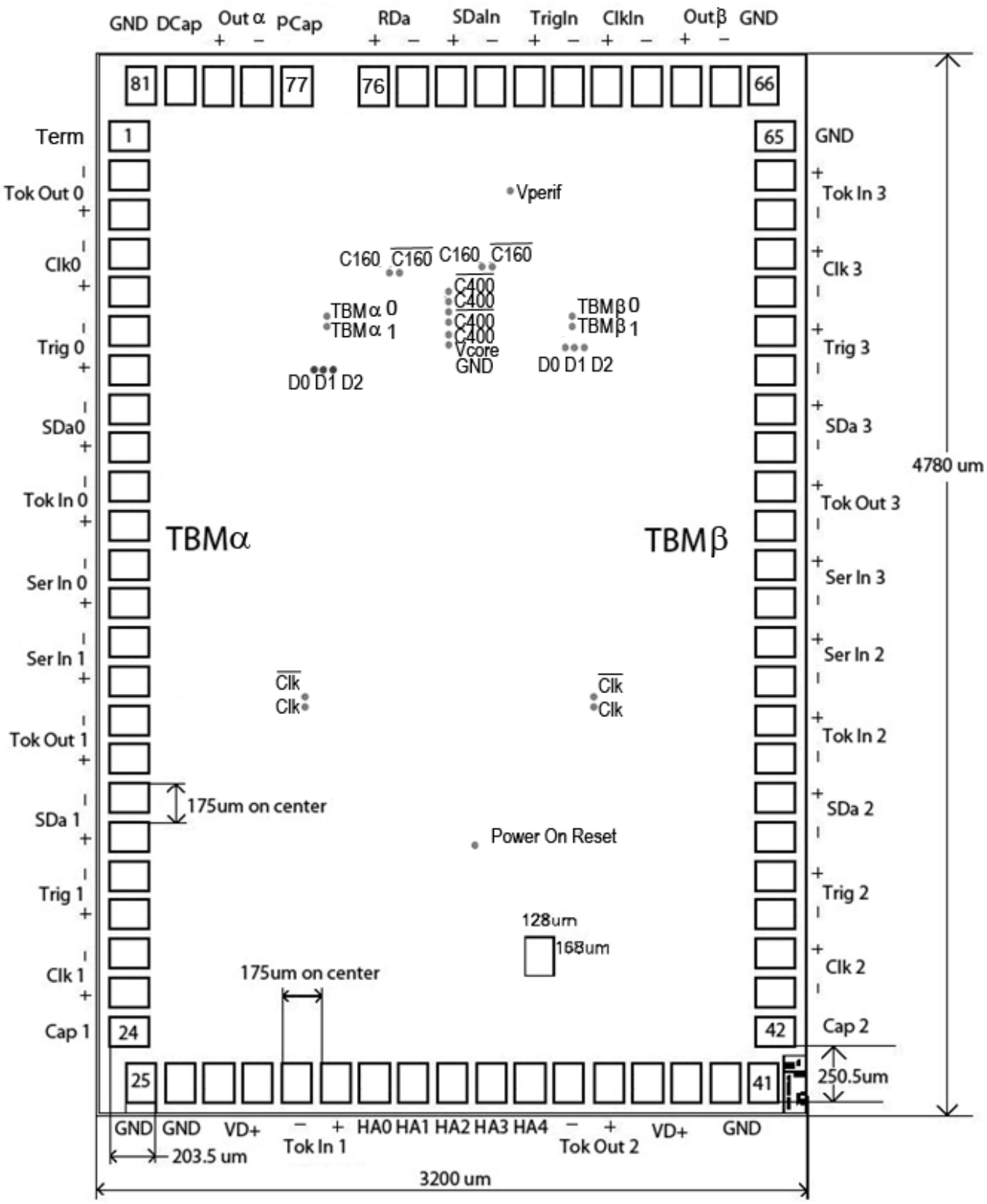
Figure 3: Trigger and Token Timing



1) Start Signal For Hub
2) Hub Address (H4, H3, H2, H1 H0)
3) Port Address (P2, P1, P0)
4) Start Signal for Readout Chip or Token Bit Manager. Note: Complimentary Bits Must Continue to be Sent During Command to ROC/TBM
5) Stop Signal to End Command to Hub
6) When inactive, Hub Should Continuously Receive Stops
7) Hub, and Port Address are Returned on RDa Line (Note: Complimentary Bits are not returned for Hub Address).

Figure 4: Serial Command Signal Timing

V. PIN DESCRIPTION



Pin #	Signal	Description
3/2	+/- Tok Out 0	Token Output
5/4	+/- CK0	Clock Out to ROC, Port 0
7/6	+/- Tr0	Trigger Out to ROC, Port 0
9/8	+/- SDa0	Serial Data Out to ROC, Port 0
11/10	+/- Tok In 0	Token Input to switch from Serial In 0 to Serial In 1
13/12	+/- SerIn 0	Serial Data In From ROC, Port 0
15/14	+/- SerIn 1	Serial Data In From ROC, Port 1
17/16	+/- Tok In 1	Token Input to switch from Serial In 0 to Serial In 1
19/18	+/- SDa1	Serial Data Out to ROC, Port 1 From TBM A
21/20	+/- Tr1	Trigger Out to ROC, Port 1 From TBM A
23/22	+/- CK1	Clock Out to ROC, Port 1 From TBM A
24	Cap 1	Bypass Cap for LVDS low level
1,25,26, 40,41,65, 66,81	GND	Power Supply Return
27,28, 38,39	VD+	Digital Power (+2.5 v) (27,28 - Periphery Power / 38,39 - Core Power)
30/29	+/- Tok In 1	Token Input to switch from Serial In 1 to Serial In 2
31	HA0	LSB of HUB Address
32	HA1	Second Bit of HUB Address
33	HA2	Third Bit of HUB Address
34	HA3	Forth Bit of HUB Address
35	HA4	MSB of HUB Address
37/36	+/- Tok Out 2	Token Output Repeats Signal from Token In 1
42	Cap 2	Bypass Cap for LVDS high level
44/43	+/- CK2	Clock Out to ROC, Port 2 From TBM B
46/45	+/- Tr2	Trigger Out to ROC, Port 2 From TBM B
48/47	+/- SDa2	Serial Data Out to ROC, Port 2 From TBM B
50/49	+/- Tok In 2	Token Input to switch from Serial In 2 to Serial In 3
52/51	+/- SerIn 2	Analog Data In From ROC, Port 2 To TBM B
54/53	+/- SerIn 3	Analog Data In From ROC, Port 3 To TBM B
56/55	+/- Tok Out 3	Token Output Repeats Signal from Token In 3
58/57	+/- SDa3	Serial Data Out to ROC, Port 3 From TBM B
60/59	+/- Tr3	Trigger Out to ROC, Port 3 From TBM B
62/61	+/- CK3	Clock Out to ROC, Port 3
64/63	+/- Tok In 3	Final Token Input, triggers sending trailer
68/67	+/- SerOutβ	Serial Data Output From TBM to FED
70/69	+/- ClkIn	System Clock Input
72/71	+/- TrigIn	Encoded Trigger Input
74/73	+/- SDaIn	Serial Command Data Input
76/75	+/- RDa	Serial Command Data returned to FEC
77	PCap	Bypass Cap for PLL Regulator
79/78	+/- SerOutα	Serial Data Output From TBM to FED
80	Dcap	Bypass Cap for Core Regulator

VI. THE TBM BEHAVIOUR.

A. Trigger signals.

The trigger signal is encoded over three clock cycles as follows: (Note: The TBM requires 2 clock cycle to pass on a trigger to the ROC, and a minimum of five more to begin outputting a Header)

- 111 – Reset the Readout Chip (RRST). This trigger is immediately passed on to the readout chip. All events on the stack are marked as No Token Pass (NTP) events. For the next eight clock cycles, all L1A triggers are also marked as NTP events, and those triggers are not passed on to the ROCs. A status bit is set in the status register for the first event following the reset, to inform DAQ a reset has occurred.
- 101 – Reset the TBM (RTBM). This trigger performs the same functions as a RRST, with the addition of resetting the TBM event counter to zero, and marking the stack as empty. If a token was out at the time of the RTBM, a trailer is sent out, after eight clock cycles.
- 100 – Pre-Calibrate/Sync/Reset (CSR). This trigger performs one of three functions, depending upon the settings of the "mode" bits of the TBM.
    - Calibrate Mode – A Calibration trigger is passed on to the ROC.
    - Sync Mode – This is treated as an L1A trigger. In addition, the lower four bits of the event counter are checked. If these bits are not equal to zero, an error bit is set in the status register, and the event counter is reset.
    - Reset Mode – The event counter is reset.

  An appropriate status bit is also set, depending

  upon the mode.
- 110 – L1A (NORMal). The event counter is incremented. If the number of entries in the stack are sixteen or less, a trigger is passed on to the ROCs. If, the number of events on the stack is greater than sixteen, the NTP bit is set in the status register. At this time, the event counter and status register are placed on the stack. However, should the stack contain thirty-two events, the event is "dropped", and a stack full bit is set in the status register, and held until a L1A occurs, and the stack has less than thirty-two events on it. (NOTE: This must be changed in TBM05. If a stack full error occurs, the status register should be cleared, prior to setting the stack full status bit).

B. Readout and Token Passing.

When an event is present on the stack, a readout sequence is initiated.

A TBM readout begins by transmitting a twelve clock cycle (160MHz) Header ID sequence (see Table 1).

The next sixteen clock cycles of the Header are used to transmit the eight bit event counter, two bits of error information, and a six bit stack count value.

Coincident with the next to last clock cycle, a Token is transmitted to the ROC (see section III: signal timing for more detail). The TBM now goes into standby mode, waiting for the last ROC in the Token chain to return the Token to the TBM.

Once the TBM Header ends, the TBM begins listening to the SerIn0 receiver. To switch from SerIn1, the Token must pulse TokIn0. In sequence, The Token must then pulse TokIn1 (to switch to SerIn2), then TokIn2 (to switch to SerIn3), finally returning to TokIn3.

Header	Trailer	Roc Header		
0	0	0	LEADER	75nS
1	1	1		
1	1	1		
1	1	1		
1	1	1		
1	1	1		
1	1	1		
1	1	1		
1	1	1		
1	1	0	ID	
0	1	Read Back Data		
0	0	Read Back Data		
Event N7	No Token Pass	Col Addr	DATA	50nS
Event N6	Reset TBM	Col Addr		
Event N5	Reset Roc	Col Addr		
Event N4	Sync Error	Col Addr		
Event N3	Sync Trigger	Col Addr		
Event N2	Clear Trig Cntr	Col Addr		
Event N1	Cal Trigger	Row Addr		
Event N0	Stack Full	Row Addr		
Data ID 1	Auto Reset Sent	Row Addr		50nS
Data ID0	Pkam Reset Sent	Row Addr		
D5	Stack Count 5	Row Addr		
D4	Stack Count 4	Row Addr		
D3	Stack Count 3	Row Addr		
D2	Stack Count 2	Row Addr		
D1	Stack Count 1	Row Addr		
D0	Stack Count 0	Pixel Hit		
Data ID 1	0	0	1	1	Pixel Hit		50nS
Data ID 0	0	1	0	1	Pixel Hit		
D5	Temp 11	Temp 05	Mode 1	TRange 05	Pixel Hit		
D4	Temp 10	Temp 04	Mode 0	TRange 04	0		
D3	Temp 09	Temp 03	DisTrigOut	TRange 03	Pixel Hit		
D2	Temp 08	Temp 02	DisTrigIn	TRange 02	Pixel Hit		
D1	Temp 07	Temp 01	Pause	TRange 01	Pixel Hit		
D0	Temp 06	Temp 00	DisPKAM	TRange 00	Pixel Hit		

Table 1:Header ID Sequence

When the Token is returned to TokIn3, the TBM transmits it's Trailer. Just like the Header, the Trailer ID is twelve clocks long. The data portion of the Trailer contains 8 bits of error status, and 8 bits that are not yet assigned. The current plan is for the those eight bit to contain either an 8 bit temperature measurement, or the data contained in

the last 8 bit TBM register accessed. If the latter, since the temperature measurement will be a TBM register, it will still be possible to include the temperature measurement in the trailer.

The TBM now contains a timeout (PKAM Counter) on the Token returning. It the Token fails to return, before the timer expires, the TBM will automatically Issue a ROC reset, ending the Token pass, deleting all data contained in the ROCs, mark all remaining events on the stack, awaiting readout as No Token Pass events, set appropriate error bits, and return the TBM trailer, 8 clocks later.

VII. Communications Control Hub.

A block diagram of the TBM08 chip is shown in Figure 4. In addition to itself, TBM08 chip also contains a Communications Control Hub.

The Hub serves as a port addressing switch for control commands that are sent from the DAQ to the Front-End TBMs and ROCs. These control commands will be sent over a digital optical link from a Front End Controller (FEC) in the electronics house to the Front-End hubs.

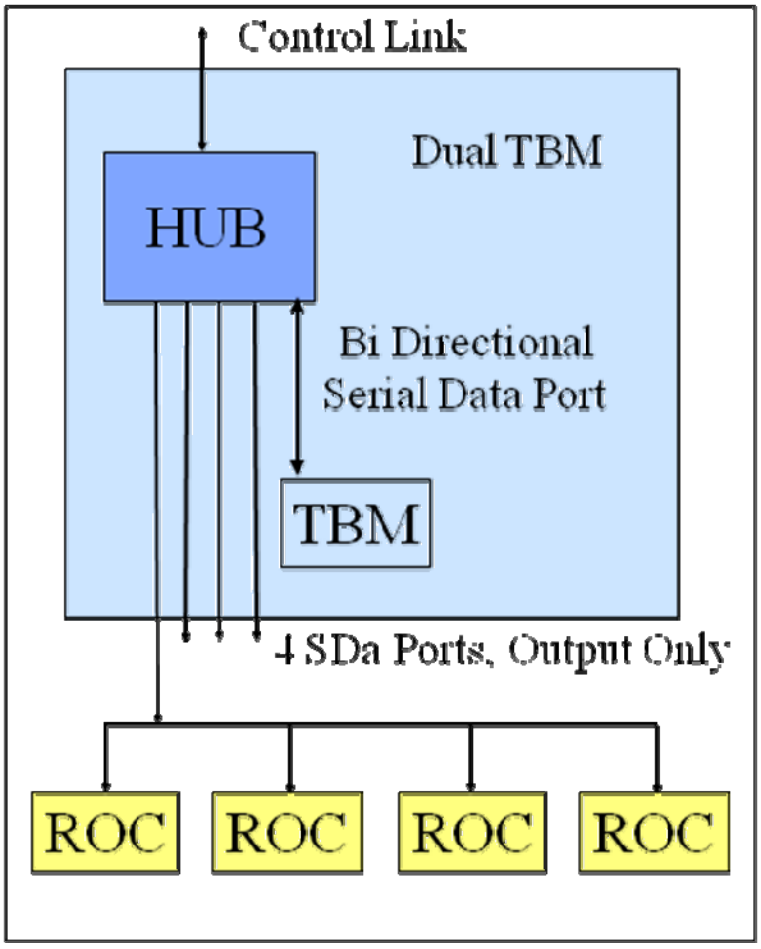


Figure 5: Block diagram of the TBM 08 chip.

The commands will be sent using a serial protocol, and run at a speed of 40 MHz. This high speed is mandated by the need to rapidly cycle through a refreshing of the pixel threshold trim bits that can become corrupted due to single

event upsets (SEU). There are four external ports on each Hub for communicating with the ROCs (ports 0 – 3) and there is one internal port for communicating with the TBMs within the chip (port 4). Sending data to Port 6, will relay the data to all four ROC ports (0 -3). Port 7 is for testing purposes, and only repeats the data back to the FEC.

The commands are broken up into 8 bit bytes, encoded into 10 clock cycles as follows:

D7 D6 D5 D4 $\overline{D4}$ D3 D2 D1 D0 $\overline{D0}$

This encoding limits the data pattern to no more than five consecutive data bits of the same value. This is necessary for the proper behaviour of the Optical Transceivers.

Each command sequence begins with a “Start” signal. A “Start” is signalled by the Serial Data line (SDa) going low, while the 40 MHz Clock line is High. Only during “Start” (and “Stop”) signalling is the Serial Data line permitted to change state while the clock line is high.

The first byte of a command will contain a 5-bit hub address and a 3-bit port address. Once a Hub is addressed, it selects the addressed port, strips off the byte containing the hub/port address and passes the remainder of the command stream unmodified onto the addressed port, as well as returning that data on the Return Data line (RDa). The Hub port remains open, transmitting all data onto the output port, until a “Stop” signal is received. In this way, control commands sent to the TBM or ROC can be of any unspecified length. A “Stop” is signalled by SDa going from low to high, while the Clock line is high. After the “Stop” is transmitted out the port, that port is closed, and the Hub then returns the Hub/Port address back to the FEC on the RDa line. Note: The returned Hub/Port address is transmitted in 8 Clock cycles, not 10 clocks.

VIII. DATAKEEPER.

The role of the Datakeeper is to combine the output data streams of two TBM cores, and encode them, using a 4 to 5 bit encoding scheme, for transmission over a fiber optic link.

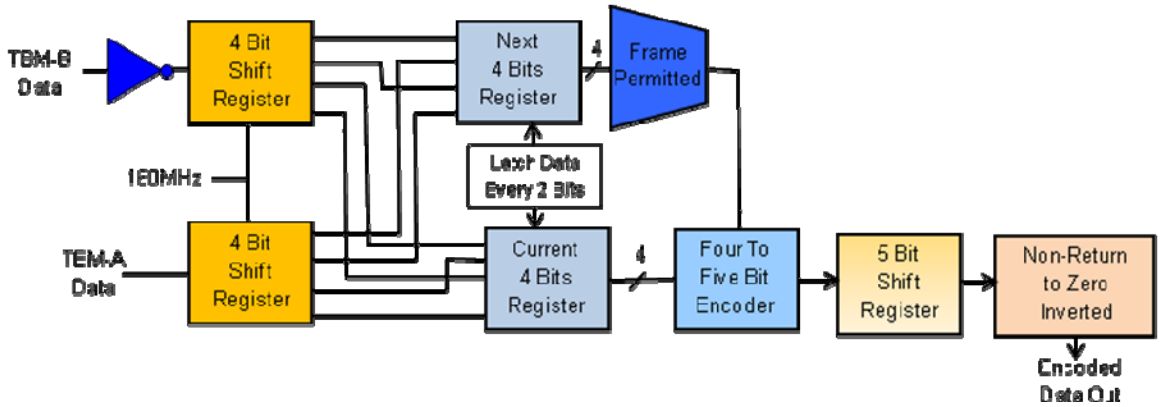


Figure 6: Block diagram of the Datakeeper.

The functions of the Datakeeper can be broken down in four stages.

- Stage 1: The output data stream from TBM-B is inverted. This is done in order that each TBM data stream can be uniquely identified at the far end of the fiber optic link (i.e If the TBM header is detected, the data stream is from TBM-A. If the Inverted TBM header is detected, the data stream is from TBM-B)

- Stage 2: Bit Interleave & Build 4-bit nibbles.

  Two 4-bit are created as follows:

  Nibble A = (1st TBM A Bit, 1st TBM B Bit, 2nd TBM A Bit, 2nd TBM B Bit)

  &

  Nibble B = (3rd TBM A Bit, 3rd TBM B Bit, 4th TBM A Bit, 4th TBM B Bit)

  Nibble A is the current nibble being encoded. Nibble B is the next nibble to be encoded.

  Nibble B is used in deciding when a Frame signal may be transmitted.

- Stage 3: Encoding & Framing.

  Nibble A is then encoded as a 5-Bit symbol using the standard 4 to 5 bit encoding table (see table 2).

4 bit Binary	Hex Value	Symbol
0000	0	11110
0001	1	01001
0010	2	10100
0011	3	10101
0100	4	01010
0101	5	01011
0110	6	01110
0111	7	01111
1000	8	10010
1001	9	10011
1010	A	10110 / 10000
1011	B	10111
1100	C	11010
1101	D	11011
1110	E	11100
1111	F	11101

Table 2: 4 to 5 Bit Encoding

Hex value 0xA is designated as a special case. There are two choices for the symbol used to represent 0xA. If Nibble A = 0xA, and if the Nibble B symbol begins with a '0', then 0xA-> 10110. Otherwise, if the Nibble B symbol begins with a '1', 0xA-> 10000. The Symbol 10000 forms a unique pattern in the data stream. This FRAMING pattern allows the FED to identify the first bit of a symbol in the final serial data stream.

- Stage 4: Non-Return to Zero Inverted (NRZI).

  Non-return to zero inverted is an encoding scheme for a serial data stream. In this system, a one is represented as a transition, from one to zero, or zero to one, depending on the previous value transmitted. A zero is represented by a lack of transition (i.e. the previous data bit is repeated).

  Table 3 illustrates how each symbol would be transmitted after NRZI.

4 bit Binary	Hex Value	Symbol	Effect of Data if 0 Precedes	NRZI Data if 1 Precedes
0000	0	11110	10100	01011
0001	1	01001	01110	10001
0010	2	10100	11000	00111
0011	3	10101	11001	00110
0100	4	01010	01100	10011
0101	5	01011	01101	10010
0110	6	01110	01011	10100
0111	7	01111	01010	10101
1000	8	10010	11100	00011
1001	9	10011	11101	00010
1010	A	10110	11011	00100
		or		
		10000	11111	00000
1011	B	10111	11010	00101
1100	C	11010	10011	01100
1101	D	11011	10010	01101
1110	E	11100	10111	01000
1111	F	11101	10110	01001

Table 3: The effect of NRZI on encoded 5-bit symbols.

Figure 7 is an example of two TBM data streams being encoded.

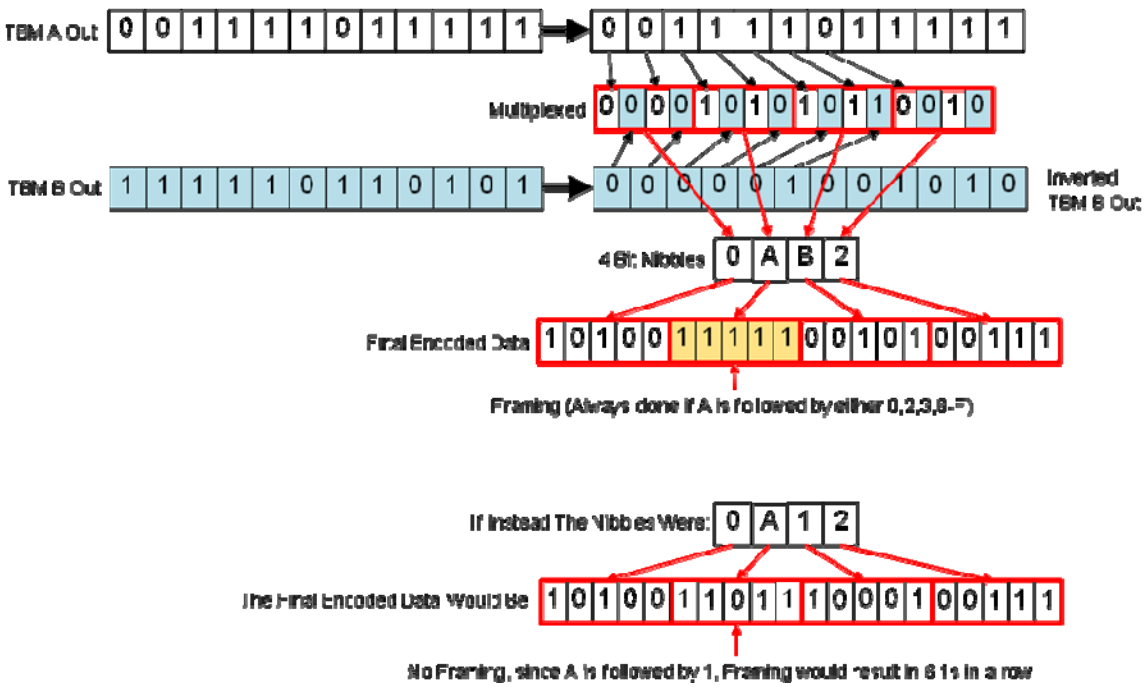


Figure 7: Encoding examples. (TBM α always is msb).

IX. PROGRAMMING TBM CONTROL REGISTERS.

An extensive set of control registers have been built into the TBM. These allow various functions and operating modes of the TBM to be controlled by issuing commands to the TBM over the control network described above. The more important of these commands are:

- Trigger Control
  - inject any trigger type
  - ignore incoming triggers
  - enable and disable the trigger output
  - change the way the TBM responds to the CSR trigger
  - issue a reset, if the token is out to long (Pkam counter)
- PKAM Counter
  - enable and disable the token out Timer
  - set the 8bit timer length (Resolution= 6.4us)
- Token Passing
  - enable and disable the token passing
- Stack Control
  - read back of the number of events on the stack
  - read back (non-destructively) of stack contents
- Readout Timing adjustments for data alignment.
  - Delay TBM Header/Trailer one 160MHz clock cycle
  - Delay Token Return by one 160MHz clock cycle
  - Adjust ROC data signals independently by 0-7ns.
- General Control
  - reset of the TBM

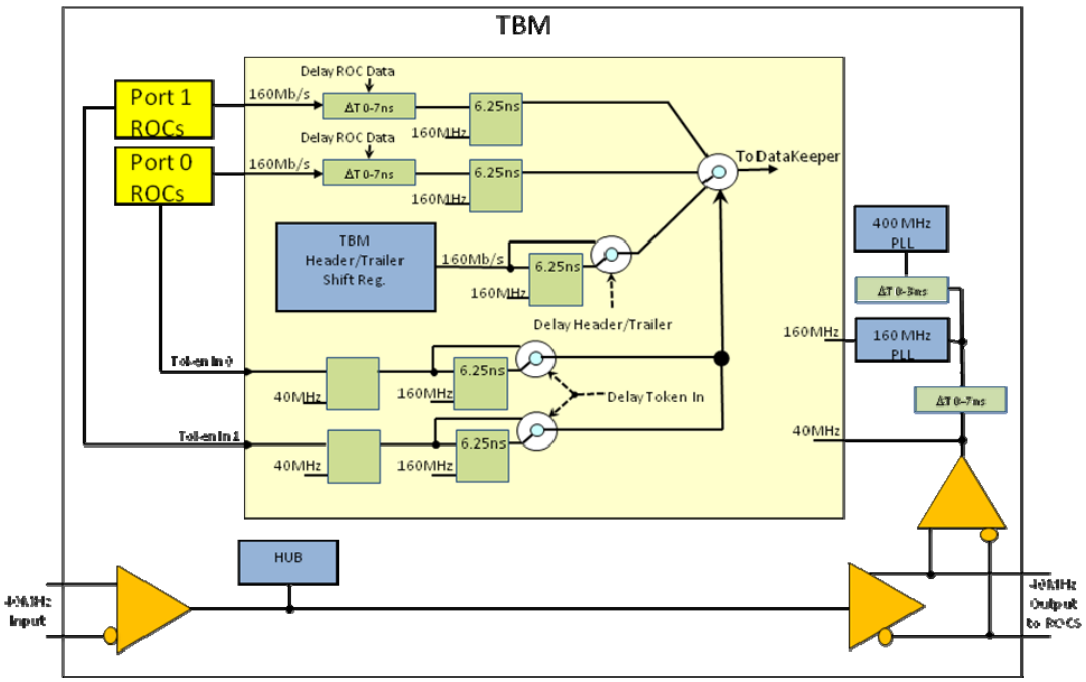


Figure 8: Block diagram of Readout delay adjustments.

Each TBM contains several control registers, accessed through Hub port 4 of the Dual TBM chip. The memory map of the control registers are as follows:

Addr (HEX)	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Base+1/0	R/w	Disable Auto Reset	Disable Trigger & Token Out (NTP)	Stack Readback Mode	Ignore Incoming Triggers	Pause Readout	Stack Full On Count = 24/32	Disable TBM Clock	Disable PKAM Counter
Base+3	R	Mode 1	Mode 0	Stack Count Bit 5	Stack Count Bit 4	Stack Count Bit 3	Stack Count Bit 2	Stack Count Bit 1	Stack Count Bit 0
Base+2	w	Mode 1	Mode 0						
Base+5	R	Stack D7 Event Num. Bit 7	Stack D6 Event Num. Bit 6	Stack D5 Event Num. Bit 5	Stack D4 Event Num. Bit 4	Stack D3 Event Num.Bit 3	Stack D2 Event Num. Bit 2	Stack D1 Event Num. Bit 1	Stack D0 Event Num. Bit 0
Base+4	W	Clear Trigger Counter	Clear Token Out	Clear Stack	Inject TBM Reset	Inject PreCal Trigger	Inject ROC Reset	Inject Sync Trigger	Inject Normal Trigger
Base+7	R	Stack D15 No Token Pass	Stack D14 TBM Reset	Stack D13 ROC Reset	Stack D12 Sync Error	Stack D11 Sync	Stack D10 CLR Trigger Counter	Stack D9 PreCal Trigger	Stack D8 Stack Full
Base+9/8	R/w	Set The Pkam Counter for TBM							
		D7	D6	D5	D4	D3	D2	D1	D0
Base+B/A	R/w	Delay Token Ins by 6.25ns	Delay Head/Trail by 6.25ns	0-7 ns Delay on Roc Data Input Port 1			0-7 ns Delay on Roc Data Input Port 0		
				D2	D1	D0	D2	D1	D0
Base+D/C	R/w	Auto Reset Setting = 256*(Setting+1) L1As							
		D7	D6	D5	D4	D3	D2	D1	D0
Base+F/E (TBM α)	R/w	160MHz	Phase	Adjust	400MHz	Phase	Adjust		
		D2	D1	D0	D2	D1	D0		
Base+F/E (TBM β)	R/w	Bits for Temperature measurement control (D5-D0 appear in TBM Trailer)							
		D7	D6	D5	D4	D3	D2	D1	D0

Stack Readout Procedure (Non Destructive):

1) Set Pause Readout, Ignore Incoming Triggers, Stack Readback Mode.
2) Read Number of Items on Stack (Stack Count)
3) Read Stack Status Bits (Stack D8 - D13).
4) Read Stack Event Number.
5) Repeat Steps 3 & 4 thirty one times.
6) Reset Pause Readout, Ignore Incoming Triggers, Stack Readback Mode.

Mode	Bit 1	Bit 0
Sync	0	X
Clr Trig Count	1	0
Calibation	1	1

Table 4: TBM Memory map. TBM α base address = 0xE0. TBM β Base Address = 0xF0

Name		Description
Disable Auto Reset		1 = Auto Reset disabled. 0 = Auto Reset enabled.
Disable Trigger Out		Disable Readout Trigger Output to ROC and Force No Token Pass For Each Event (Calibration and Reset Triggers are still Output to ROC)
Stack Read back Mode		Allow Stack Read back.
Ignore Incoming Triggers		Ignore all signals on TrigIn Line (used with Stack Read back Mode)
Pause Readout		TBM will not Begin Readout/Token Pass Cycle (used with Stack Read back Mode)
Stack Full On Count = 24/32		1 = Stack is limited to 24 entries. 0 = Stack is limited to 32 entries.
Disable TBM Clock		Disable Clock within TBM except Control registers. Also Disables Output Clocks.
Disable Pkam Counter		1 = Pkam counter disabled. 0 = Pkam counter enabled.
Mode Setting		
Mode 1	Mode0	(See Trigger Definition for Pre-Calibrate/Sync/Reset (CSR).)
0	X	Sync
1	0	Clear Event Counter
1	1	Pre - Calibration
Stack Count Bits 0 - 5		Reading these bits returns the number of entries currently on the Stack
Stack Event Number Bits 0 - 7		Reading these bits returns the current Event Number on the Stack, and increments the Stack Read Pointer. Should Only Be Accessed in Stack Read back Mode!
Clear Event Counter		Set Event Counter To 0
Clear Token Out		If the TBM is waiting for the Token, tell it the Token has returned, and issue a Trailer
Clear Stack		Set the Stack Count, and the Stack Read & Write Pointers to zero.
Inject TBM Reset		The TBM issues an Internal TBM reset. (See Trigger Signals Section)
Inject Pre-Calibrate Trigger		The TBM issues an Pre-Calibrate Trigger to the ROC, independent of the TBM Mode Setting.
Inject ROC Reset		The TBM issues an Internal ROC reset. (See Trigger Signals Section)
Inject Sync Trigger		The TBM issues an Internal Sync Trigger to itself, independent of the TBM Mode Setting.
Inject Normal Trigger		The TBM issues an Internal Normal reset. (See Trigger Signals Section)
Stack - No Token Pass		Reading these bits returns the current No Token Pass Status Bit on the Stack
Stack - TBM Reset		Reading these bits returns the current TBM Reset Status Bit on the Stack
Stack - ROC Reset		Reading these bits returns the current ROC Reset Status Bit on the Stack
Stack - Sync Error		Reading these bits returns the current Sync Error Status Bit on the Stack
Stack - Sync		Reading these bits returns the current Sync Trigger Status Bit on the Stack
Stack - CLR Trigger Counter		Reading these bits returns the current Clear Event Counter Trigger Status Bit on the Stack
Stack - Pre-Calibrate Trigger		Reading these bits returns the current Pre-Calibrate Status Bit on the Stack
Stack - Stack Full		Reading these bits returns the current Stack Full Status Bit on the Stack

Table 5a: TBM Control Register Definitions

Name	Description
Pkam Counter	Set an 8 bit counter, for the maximum time to readout a single event. Each count = 6.4us. A ROC reset is issued, if the readout exceeds the Timeout
Delay Token In by 6.25ns	Delay Switching of TBM output Mux by 1 160MHz clock. Use if last bit of ROC data is cut off
Delay Head/Trail by 6.25ns	Delay TBM Header and Trailer by 160MHz clock. Use if there is an extra clock data bit between the end of the Header, and the start of ROC Data.
0-7 ns Delay on ROC Data input Port 1.	Delay ROC data input by 0-7ns on Port 1. In one ns increments.
0-7 ns Delay on ROC Data input Port 0.	Delay ROC data input by 0-7ns on Port 0. In one ns increments.
Auto Reset Setting	Reset ROCs every N L1As. Where N is 256 times (8bit Number + 1).
160 MHz Phase Adjust	Adjust Phase relationship between 40 MHz & 160 MHz,400 MHz in 1ns increments
400 MHz Phase Adjust	Adjust Phase relationship between 160 MHz & 400 MHz in 0.4ns increments
Temperature Measurement	8 Bits assigned to future Temperature measurement control. Bits D5-D0 appear in TBM Header.

Table 5b: TBM Control Register Definitions

A. Programming Examples.

Programming a TBM control register requires three bytes be encoded serially, and transmitted as follows:

Start (Hub/Port Address) Start (TBM Register Address) (Data Byte) Stop

The TBM returns:

Start (TBM Register Address) (Data Byte) Stop (Hub/Port Address*)

(* Hub/Port Address does not use the 10 bit encoding in return data)

Example 1)

Set TBM A Readout Speed to 40 MHz. (Note: Extra bits added for 10 Bit Encoding Marked in Red)

Hub Address 10
Port Address 4
TBM Register Address 0xe0
Serial Programming Sequence:
Start 0101 0 0100 1 Start 1110 1 0000 1 0000 1 0001 0 Stop

Returned Data Sequence:

Start 1110 1 0000 1 0000 1 0001 0 Stop 01010100 Stop

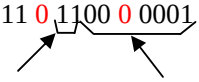
Example 2)

Read TBM B Trigger Mode.
Hub Address 10
Port Address 4
TBM Register Address 0xf3

Serial Programming Sequence:
Start 0101 0 0100 1 Start 1111 0 0011 0 1111 0 1111 0 Stop
NOTE: When READING data from the TBM, a data byte of all 255 must be sent out.

Returned Data Sequence:

Start 1111 0 0011 0 1100 0 0001 0 Stop 01010100 Stop



Calibration Mode. One Event On Stack

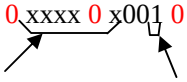
Example 3)

Read TBM B Force Readout Clock On Bit.
Hub Address 10
Port Address 4
TBM Register Address 0xf9

Serial Programming Sequence:
Start 0101 0 0100 1 Start 1111 0 1001 0 1111 0 1111 0 Stop

Returned Data Sequence:

Start 1111 0 1001 0 xxxx 0 x001 0 Stop 01010100 Stop



These bits are not defined. Readout Clock Not Forced On

Example 4)

Sequence of Commands to Read Back the Stack Contents. (Order is important)

Step 1) Set Pause Readout, Ignore Incoming Triggers, Stack Read Back Mode Bits.
This prevents the Stack from being altered during read back.

Step 2) Read Number of Items on Stack (Stack Count).
To determine the number of events waiting on the Stack.

Step 3) Read Stack Status Bits (Stack D15 – D8)

Step 4) Read Stack Event Number (Stack D7 – D0)

Step 5) Repeat Steps 3 & 4 thirty one times.
This Reads the remaining 31 events and returns the Stack to its initial state.

Step 6) Reset Pause Readout, Ignore Incoming Triggers, Stack Read