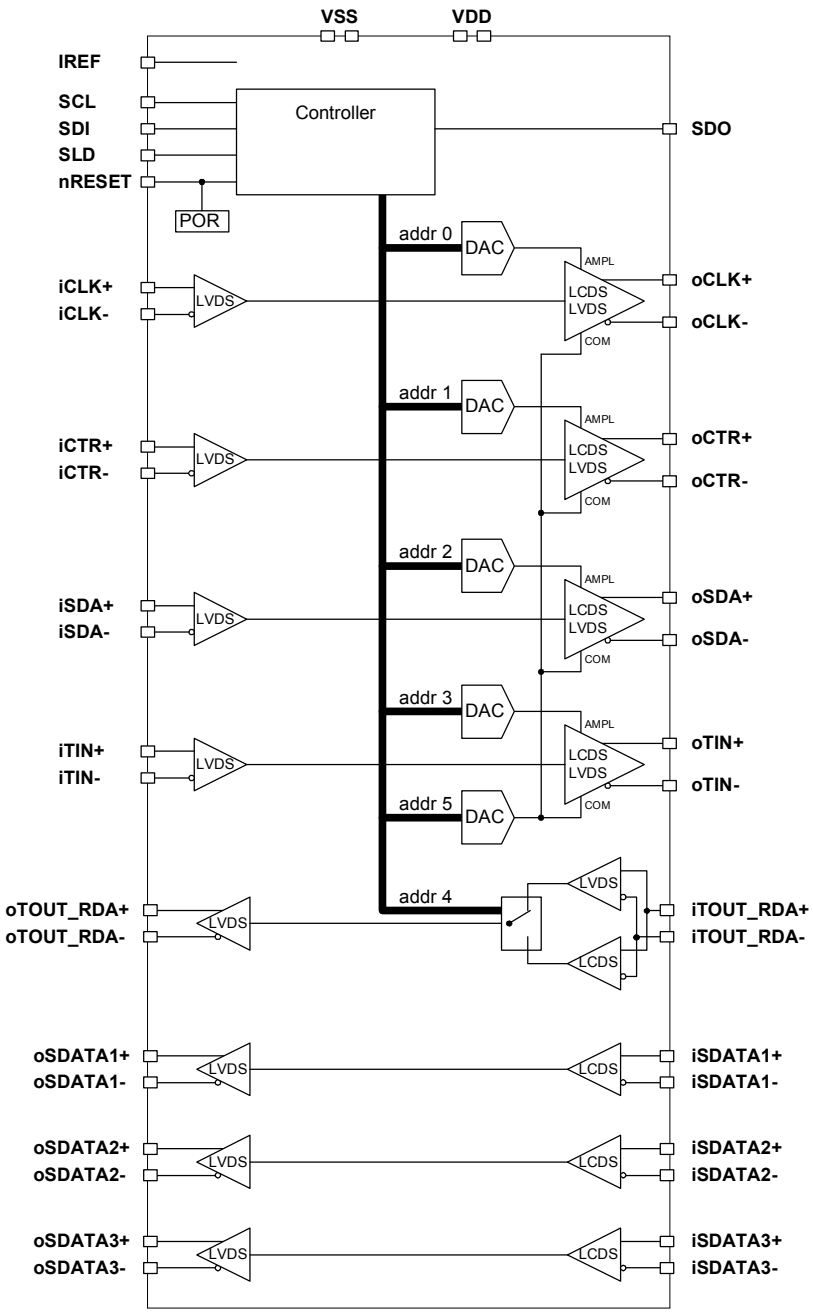
Configurable LVDS to LCDS Interface

Description

The LCDS2LVDS is designed for the CMS pixel detector test board (PixelDTB). It acts as a level translator between the LVDS levels of the test system (FPGA) and the LCDS/LVDS signals of the DUT (Module or ROC).

Features

- Full set of differential drivers and receivers to provide all module and ROC signals
- LVDS signals to test system (FPGA)
- Individual adjustable driver amplitude to DUT
- Configurable LVDS/LCDS driver for DUT
- Driver common mode adjust
- Serial interface for configuration
- Stand alone operation without using the serial interface (only default driver settings)

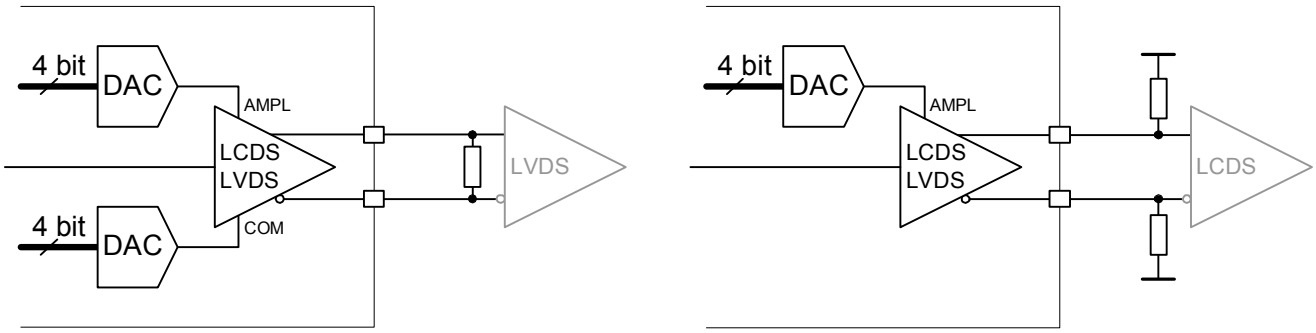


Pin description

Signal	*Description*
VSS	Power Ground
VDD	Power +2.5V
IREF	External bias input. Connect with 200 kΩ Ohm resistor to VDD
nRESET	Active low reset. Is driven by the internal power on reset circuit (POR) circuit. If this pin is driven external use an open drain driver to VSS.
SCL	Serial clock input for configuration (see “serial configuration protocol”)
SDA	Serial data input for configuration (see “serial configuration protocol”)
SLD	Serial load input for configuration (see “serial configuration protocol”)
SDO	Serial data output (see “serial configuration protocol”)
iCLK +/-	LVDS “clock” signal from test system
oCLK +/-	Adjustable LCDS/LVDS “clock” to DUT
iCTR +/-	LVDS “cal_trig_res” signal from test system
oCTR +/-	Adjustable LCDS/LVDS “cal_trig_res” signal to DUT
iSDA +/-	LVDS “i2c data” signal from test system
oSDA +/-	Adjustable LCDS/LVDS “i2c data” signal to DUT
iTIN +/-	LVDS “token in” signal from test system
oTIN +/-	Adjustable LCDS/LVDS “token in” signal to DUT (only ROC)
oTOUT_RDA +/-	LVDS “token out” output from ROC or “rda” from module to the test system
iTOUT_RDA +/-	LVDS “token out” from ROC or LCDS “rda” from module
oSDATAn +/-	LVDS data signal to the test system (n = 1, 2, 3)
iSDATAn +/-	LCDS data signal from DUT (n = 1, 2, 3)

Driver configuration

The combined LCDS/LVDS driver can generate LVDS or LCDS signals depending on the line termination. To get LVDS signals the termination resistor has to be placed between the differential line pairs. The amplitude and the common mode have to be adjusted by the serial programming interface to LVDS specifications.
In LCDS mode, two termination resistors have to be placed to VSS (ground). The amplitude should be adjusted to the LCDS level. The common mode adjust has no influence in this configuration. After power on reset the driver is configured to LCDS levels.



Serial Configuration Protocol

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Dimensions and Pin Assignment