Gatekeeper 06 Chip Documentation

Version 1.00

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I. INTRODUCTION

The Gatekeeper performs two essential functions in the pixel system. First, the Gatekeeper translates signals from the Digital Opto-Hybrid / Phase Locked Loop LVDS standard to the Fan Chip / TBM LCDS standard, and does the reverse for the return signals. Second, as the name suggests, the Gatekeeper opens and closes a gate between the Opto-Hybrid / PLL and the Front end electronics.

II. GATEKEEPER BEHAVIOUR.

By default and after reset, the gate of the Gatekeeper is closed.

When closed, the Serial Data Line (SDa) "can" be blocked from being sent on to the front end chips, but the System Clock (Clk) and Cal/Trigger/Reset (CTR) lines are always sent on to the Front end. Additionally, the Clk and SDa lines are connected to the Return Clock (RCLk) and Return Data (RDa) lines respectively, to keep the return Optical Links active. As shown in Figure 1, the Clk, CTR & SDa lines have an internal fixed delay of ~8 ns from chip input to chip output. This delay allows the START/STOP circuit time to determine a start condition (i.e. The SDa line transitions from High to Low while the Clk line is High) and open the Gate, before the start condition has passed through the fixed delay to the output Drivers.

Once the Gate is open, all data on the SDa_In line is passed on to the SDa_Out. The return data on the RDa_In line is connected to the RDa_Out Line. The RClk line gets it's signal either from the return clock input (RClk_In) of from the Clk line, after it passes through an adjustable delay line, depending on a mode setting pin. When a stop condition is detected (A stop consists of the SDa line transitioning from Low to High, while the Clk line is High), the Gatekeeper waits for 10 clock cycle (long enough for the Hub to return its address) and then closes the gate.

There are two Mode select pins:

1) EnSDAOut – A High keeps the SDa Gate open, so all data received by the Gatekeeper is passed on to the front end. This would allow the TBM to continuously receive stop signals.
2) EnRlkIn – A High selects the TBM RCl to be sent back to the Front end controller when the gate is open. A Low selects that the Clk signal, delayed by an adjustable delay line (18ns max, 16 steps) is sent to the Front end controller when the gate is open.

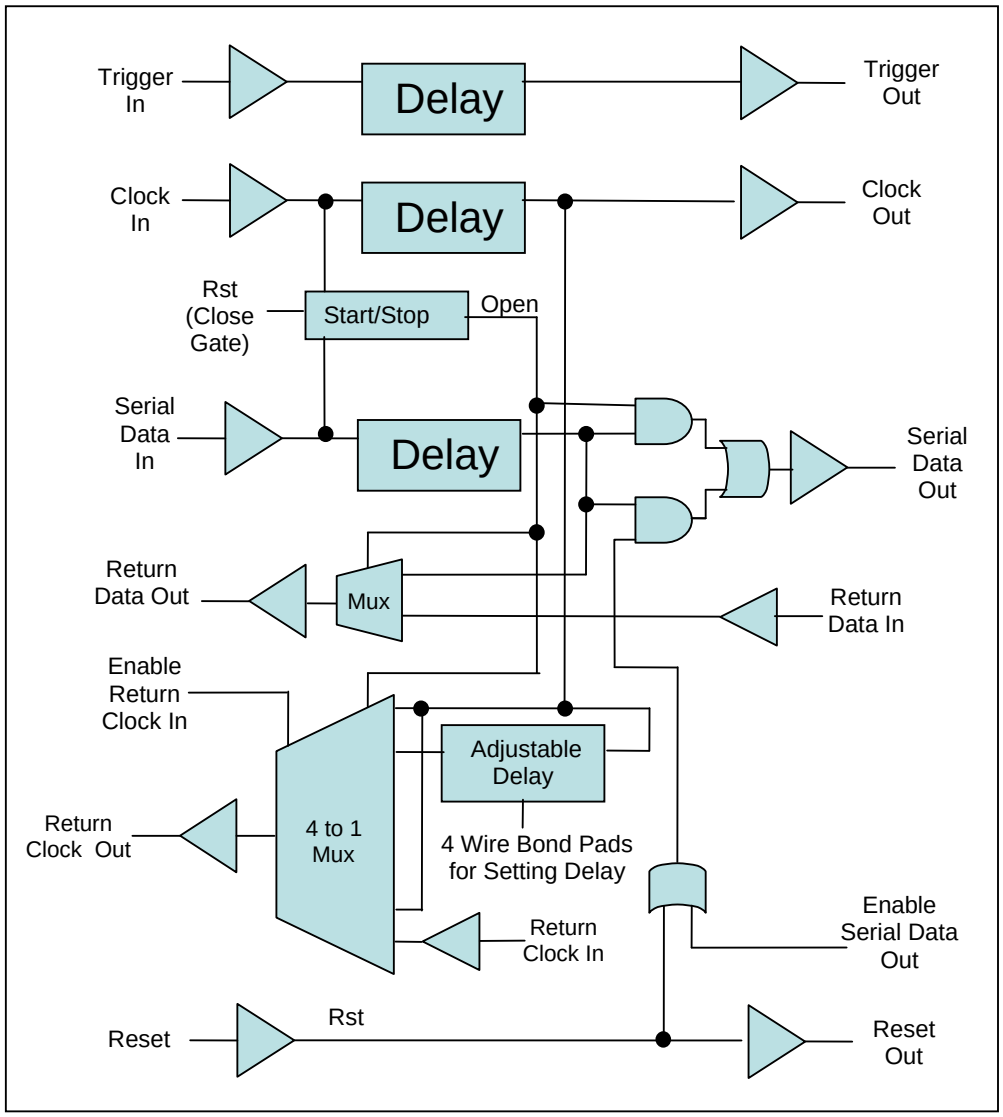


Figure 1: Functional block diagram of the Gatekeeper 05

III. ELECTRICAL CHARACTERISTICS

Supply Voltage (Vdd) +2.5 v

Power Consumption * TBD

Front End Control Signals **Single Ended**			
Reset (Rst)	ViH = 2.5v	ViL = 0v	Active Low (weak transistor Pullup)
Adjustable Delay Settings (A0-A3)	ViH = 2.5v	ViL = 0v	75k ohms internal Pulldown
EnRckIn	ViH = 2.5v	ViL = 0v	Active Low (weak transistor Pullup)
EnSDaOut	ViH = 2.5v	ViL = 0v	Active Low (weak transistor Pullup)
Double Ended **Inputs**			
Clock In (Clk_In)	VoH = 1.2v	VoL = 1.0v	100 ohms differential termination required
Serial Data In (SDa_In)	VoH = 1.2v	VoL = 1.0v	100 ohms differential termination required
Trigger In (CTR_In)	VoH = 1.2v	VoL = 1.0v	100 ohms differential termination required
Outputs			
Serial Data Out (RDa_Out)	VoH = 1.2v	VoL = 1.0v	(Termination must not be used here)
Data Clock Out (RClk_Out)	VoH = 1.2v	VoL = 1.0v	(Termination must not be used here)
Fan/TBM Signals Double Ended			
Outputs			
Serial Data Out (SDa_Out)	IiH = 3.3ma	IiL = 0.2ma	36 ohms to gnd required on each pin
Clock Out (Clk_Out)	IiH = 3.3ma	IiL = 0.2ma	36 ohms to gnd required on each pin
Trigger Out (CTR_Out)	IiH = 3.3ma	IiL = 0.2ma	36 ohms to gnd required on each pin
Inputs			
Return Clock Input (RClk_In)	IiH = 3.3ma	IiL = 0.2ma	36 ohms to gnd required on each pin
Return Data Input (RDa_In)	IiH = 3.3ma	IiL = 0.2ma	36 ohms to gnd required on each pin
Capacitor Pins (for internal regulator bypassing)			
Cap	2.1 v		0.1uF Nominal

IV. SIGNAL TIMING

Note: SDaOut Signal is bandwidth limited for clarity.

A. Effect of EnSDaOut signal on Gatekeeper

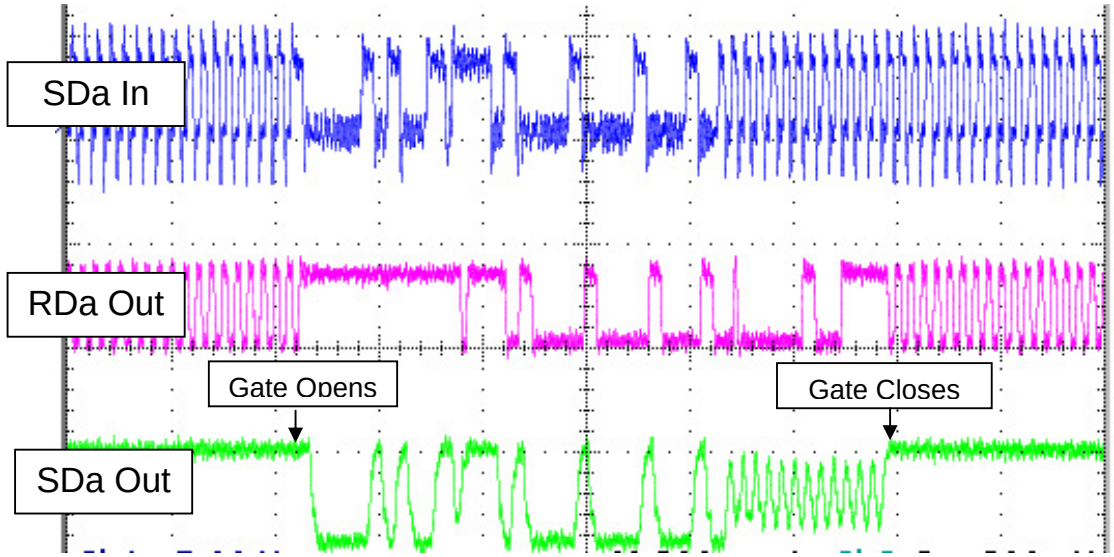


Figure 2: EnSDaOut=low. SDaOut is high when gate is closed. RDaOut Follows RDaIn when gate is open and SDaIn when gate is closed.

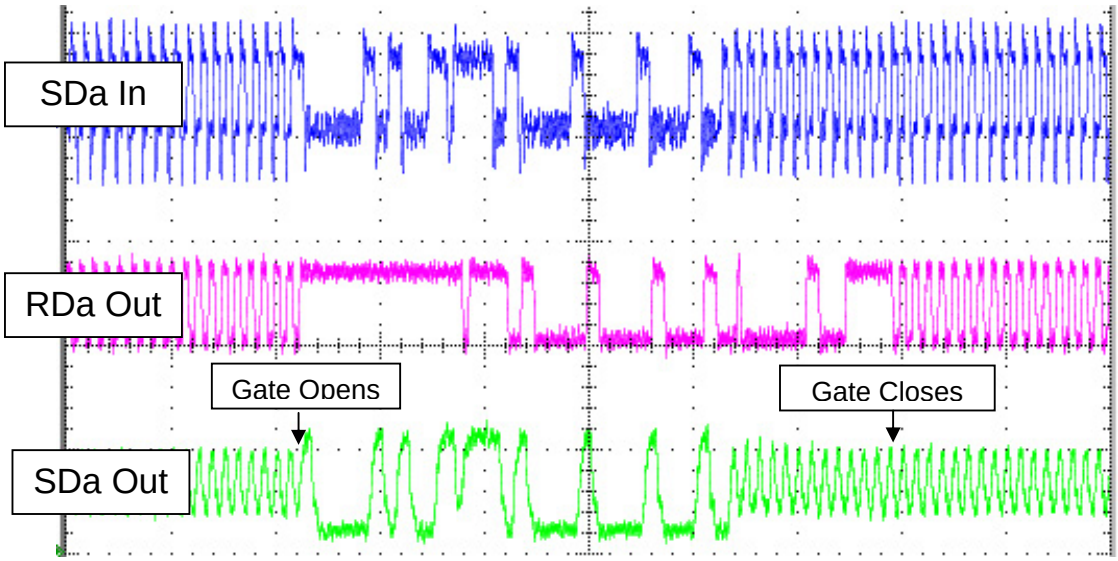


Figure 3: EnSDaOut=high. SDaOut always follow SDaIn

B. Effect of EnRckIn signal on Gatekeeper

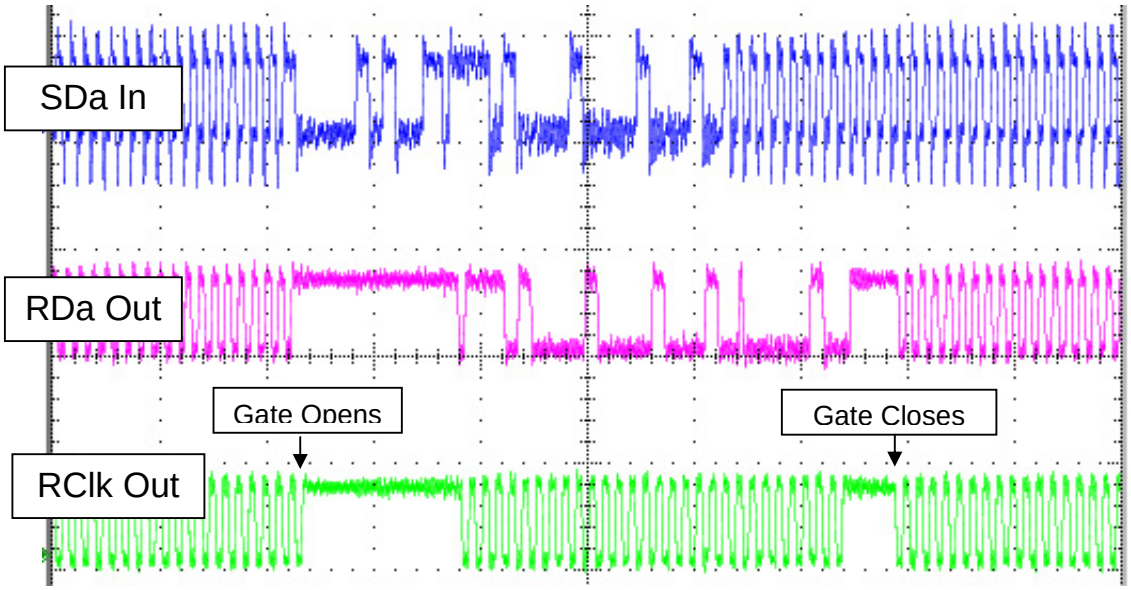


Figure 4: EnRckInt=high. RClkOut follows RClkIn when gate is open and ClkIn when gate is closed.

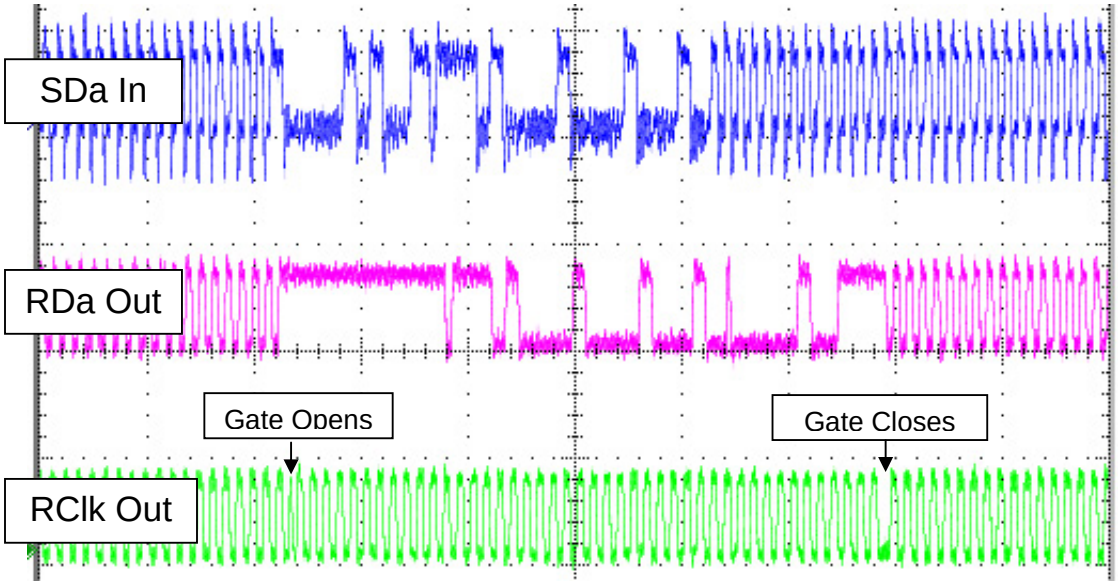
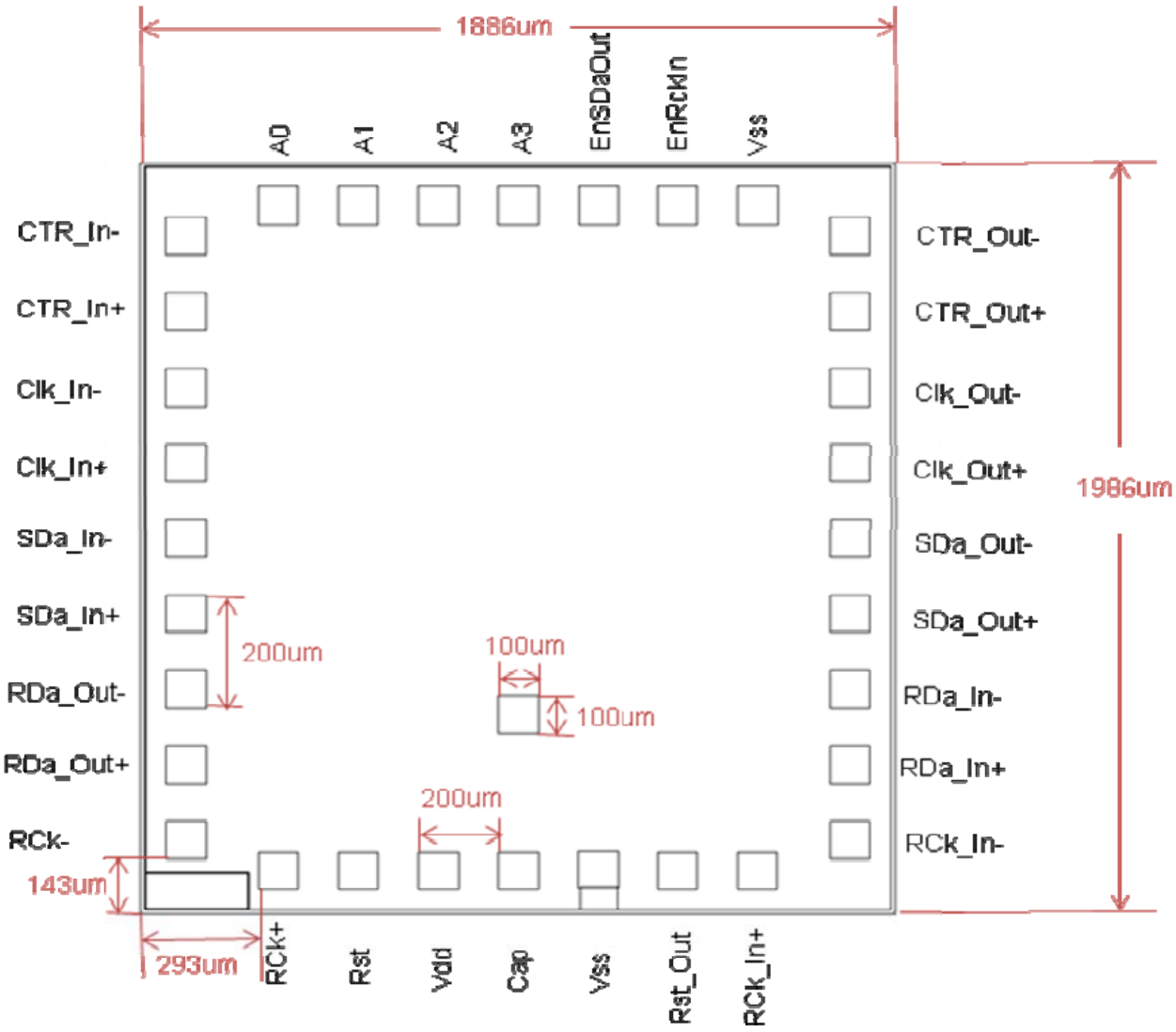


Figure 5: EnRckInt =low. RClkOut follows ClkIn when gate is open and ClkIn when gate is closed.

V. PIN DESCRIPTION & DIMENSIONS



Dimensions are all in microns.

Pin #	Signal	Description
1/32	+/-CTR_In	Cal/Trigger/Reset Signal from FEC
3/2	+/- Clk_In	Clock Signal from FEC
5/4	+/- SDa_In	Serial Data Signal from FEC
7/6	+/- RDa_Out	Return Serial Data Signal to FEC
9/8	+/- RClk_Out	Return Clock Signal to FEC
10	Rst	Reset Signal Input (Active Low Signal closes gate)
11	VDD	Digital Power (+2.5 v)
12	Cap	Bypass Cap for Digital Regulator
13,25	VSS	Power Supply Return
14	Rst_Out	Buffered Reset Signal Output
15/16	+/- RClk_In	Return Clock Input Signal from FanIn/TBM
17/18	+/- RDa_In	Return Serial Data Input Signal from FanIn/TBM
19/20	+/- SDa_Out	Serial Data Output Signal to FanIn/TBM
21/22	+/- Clk_Out	Clock Output Signal to FanIn/TBM
23/24	+/- CTR_Out	Cal/Trigger/Reset Signal to FanIn/TBM
26	EnRckIn	High = TBM RCl Connected to RClk_Out when the gate is open. (Default) Low = Adjustable delayed Clk is Connected to RClk_Out when the gate is open.
27	EnSDaOut	High = SDa Out Follows SDa In, regardless of gate status. (Default) Low = SDa Out is Pulled High when gate is closed.
28	A3	MSB of Adjustable Internal Delay line for RClk_Out (18ns max, 16 steps)
29	A2	Third Bit of Adjustable Internal Delay line for RClk_Out (18ns max, 16 steps)
30	A1	Second Bit of Adjustable Internal Delay line for RClk_Out (18ns max, 16 steps)
31	A0	LSB of Adjustable Internal Delay line for RClk_Out (18ns max, 16 steps)